

UNCLASSIFIED

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 11
AUGUST 1948

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SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
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SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts
Project DIC 6345

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TABLE OF CONTENTS

	Page
FORWORD	1
Project Whirlwind	
The Whirlwind Computers	
Reports	
GENERAL STATUS	2
SUMMARY SCHEDULE	3
LONG TERM WHIRLWIND SCHEDULE	9
STORAGE TUBES	11
General Status	
Television Setup	
GATE TUBE CHAIN PERFORMANCE	12
MATHEMATICS	13
Simultaneous Linear Algebraic Equations	
Integral Equations	
Differential Equations	
Representation of Empirical Functions	
TELETYPE INPUT-OUTPUT DEMONSTRATOR	14
VISITS	15
Visitors to the Laboratory	
Visits by Project Staff Members	
APPENDIX	17
Reports and Publications	

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

Installation of the WWI computer has been started. Racks in the power supply room and computer room are being assembled for the first of the power supplies to arrive in September, and for the A-register of the arithmetic element to arrive in October.

The difficulties in evaporation of storage tube mosaics as reported in July have been overcome. The first 5-inch-diameter storage tube with a beryllium mosaic storage surface was completed; results were favorable for a first tube. See the article on Storage Tubes.

A temporary control room is planned for the WWI installation period. A final control desk and indicators for operating and trouble-locating equipment will be designed later based on preliminary installation experience.

In recent months a number of modifications of the original basic circuits have been made, some of them as a result of the change from 6AG7 to 7AD7 tubes, others in the interest of simplification, elimination of unnecessary components, and improvement of performance.

LONG-TERM TIME SCHEDULE

New detailed schedules, up to date for July and published last month, are posted in this issue to the end of August. The absence of long-term perspective in these detailed reports has in the past resulted in some confusion and misunderstanding. It has not been possible for the reader to relate the current work to that already completed or to that yet to be finished.

To present the proper setting for current activity, a long-range schedule is included in this

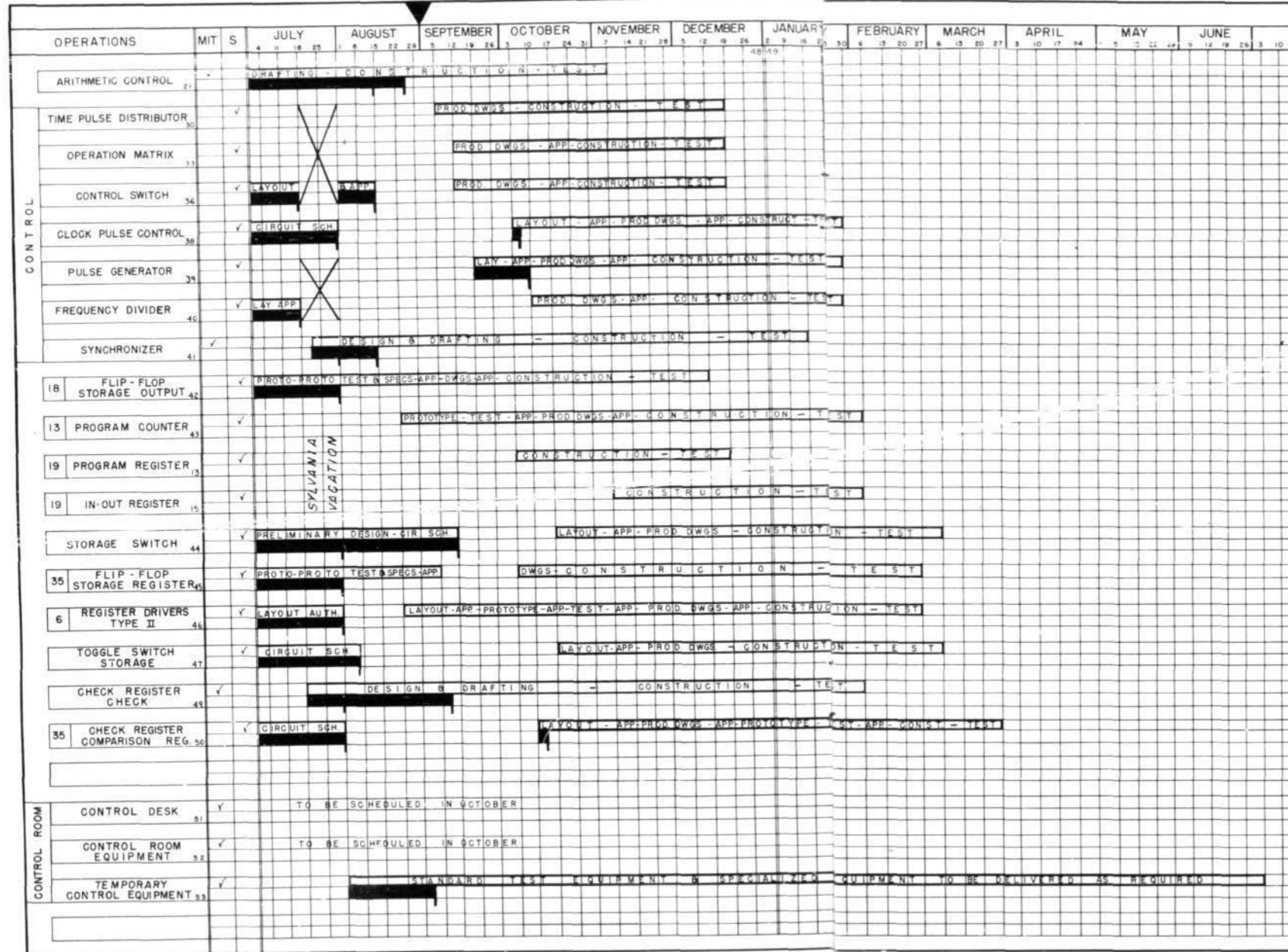
Summary Report. It extends from the initiation of the project in 1944 through the final testing of the WWI prototype high-speed electronic computer but does not show the period of computer application which must await a more complete specification of objectives and scope of such application.

The schedule reflects a revised basis for making time estimates. In the past, time schedules have assumed a continually growing staff and increased subcontracting. Because present plans are to hold expenditures at the August level (partially due to lack of additional floor space), the schedules are now based on progress at the present rate rather than at an increased future rate.

The first detailed time schedules were prepared in January, 1948. Those schedules showed most of WWI to exist at the end of 1948. As discussed in the July report this was revised to the end of 1949 based on the progress in the first six months and on the order in which the computer parts could be assembled. The accompanying long-term schedule is further revised to the end of 1950. This last extension of one year may be partially recovered, but now is indicated by the new assumptions of available staff, floor space, and subcontracting. It will be noted that current work is approximately midway between the initiation of the project in 1944 and the end of the installation and the study of checking and trouble location methods in 1951.

The present level of work does not provide adequate preparation for computer applications. Additional auxiliary equipment will be required for simulation or control investigations, and additional input-output equipment will be required for effective and efficient application to engineering computation. Insufficient provision is made for applications studies and investigations to establish the value and relationship of digital computers to other military and civilian activities.

SUMMARY - WHIRLWIND I SCHEDULES CONT.



LEGEND



Period of one month, comprising the total number of days in the month.



Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.



Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.



Date of latest posting.



Summary line. Shows overall status of the project.



Column showing whether M.I.T. or Sylvania will do major portion of the job.

SUMMARY - WHIRLWIND I SCHEDULES -CONT.

OPERATIONS	MIT	S	JULY							AUGUST							SEPTEMBER							OCTOBER							NOVEMBER							DECEMBER							JANUARY							FEBRUARY							MARCH							APRIL							MAY							JUNE						
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31																																																					
FILM READER-RECORDER 84	EASTMAN		COMPLETE	BROADBAND TEST-FINAL DESIGN							CONSTRUCTION							ASSEMBLY TEST DELIVERY 4 UNITS																																																																				
INPUT-OUTPUT CONTROL 85	KODAK	✓									BLOCK DIAGRAM														DESIGN & CONSTRUCTION																																																													
KEYBOARD & PRINTING CONTROL 86		✓									BLOCK DIAGRAM																					DESIGN & CONSTRUCTION																																																						
TEST EQUIPMENT 87		✓	CONSTRUCTION OF TEST EQUIPMENT AS REQUIRED																																																																																			
TROUBLE LOCATION METHODS 88		✓	FURTHER STUDY OF BASIC METHODS							APPLICATION OF METHODS							TO ARITH. ELEM. APPLICATION TO CENTRAL CONT.																																																																					
AIR CONDITIONING 89	CARRIER CORP.		ERECT ROUSE							INSTALL EQUIP.																																																																												
PREPARATION OF COMPUTER ROOM 90		✓	PAINTING & RADIATOR REMOVAL																																																																																			
OUTPUT CIRCUITS 92		✓								SPECIFICATIONS FOR WWI							DESIGN							PROTOTYPE							CONSTRUCTION																																																							
DEFLECTION CIRCUITS 93		✓								COMPLETE TEST OF PROTOTYPE							FINAL DESIGN AND TEST							CONSTRUCTION							INSTALL																																																							
CONTROL CIRCUITS 94		✓								PRELIM. BLOCK DIAGRAM							FINAL BLOCK DIAGRAM							DESIGN AND CONSTRUCTION																																																														
5 INCH TUBES 95		✓	2 TUBES EACH OF BE MOSAIC & CAL. TUNG. FOR 6X6 ARRAY - 2 TUBES OF BE MOSAIC FOR 16X16 ARRAY																																																																																			
EXPAND VACUUM LABORATORY FACILITIES 96		✓	RECORDING INSTRUMENTS - HIGH SPEED EXHAUST SYSTEM - AUTO. PROCESSING CONTROL																																																																																			
EXPAND TEST LABORATORY FACILITIES 97		✓	TV UNIT - AUTO READ - WRITE - OUTPUT CIRCUITS - LIFE & RELIABILITY																																																																																			
STORAGE PHENOMENA RESEARCH 98		✓	BE MOSAIC STABILITY - CAL. TUNG. STABILITY																																																																																			
STABILITY RESEARCH TUBES & STUDIES 99		✓	BE STRIP TUBES - CONCENTRIC RING TUBES - HOLDING BEAM VELOCITY DISTRIBUTION																																																																																			
ELECTROSTATIC GUNS 100		✓	MISC. GUN STUDIES & DESIGN AS REQ.																																																																																			
LIFE & RELIABILITY TESTS 101		✓								PLA TESTS							PROCURE EQUIPMENT							MAKE TESTS																																																														
EQUIP FOR PILOT QUANT. TUBE CONSTRUCTION 102		✓															DESIGN & CONSTRUCT																																																																					
FINAL DESIGN FOR FIRST WWI TUBES 103		✓															DESIGN							PILOT CONSTRUCTION																																																														
CONSTRUCTION OF WWI TUBES 104		✓																													CONSTRUCT																																																							

LEGEND



Period of one month, comprising the total number of days in the month.



Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.



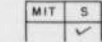
Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.



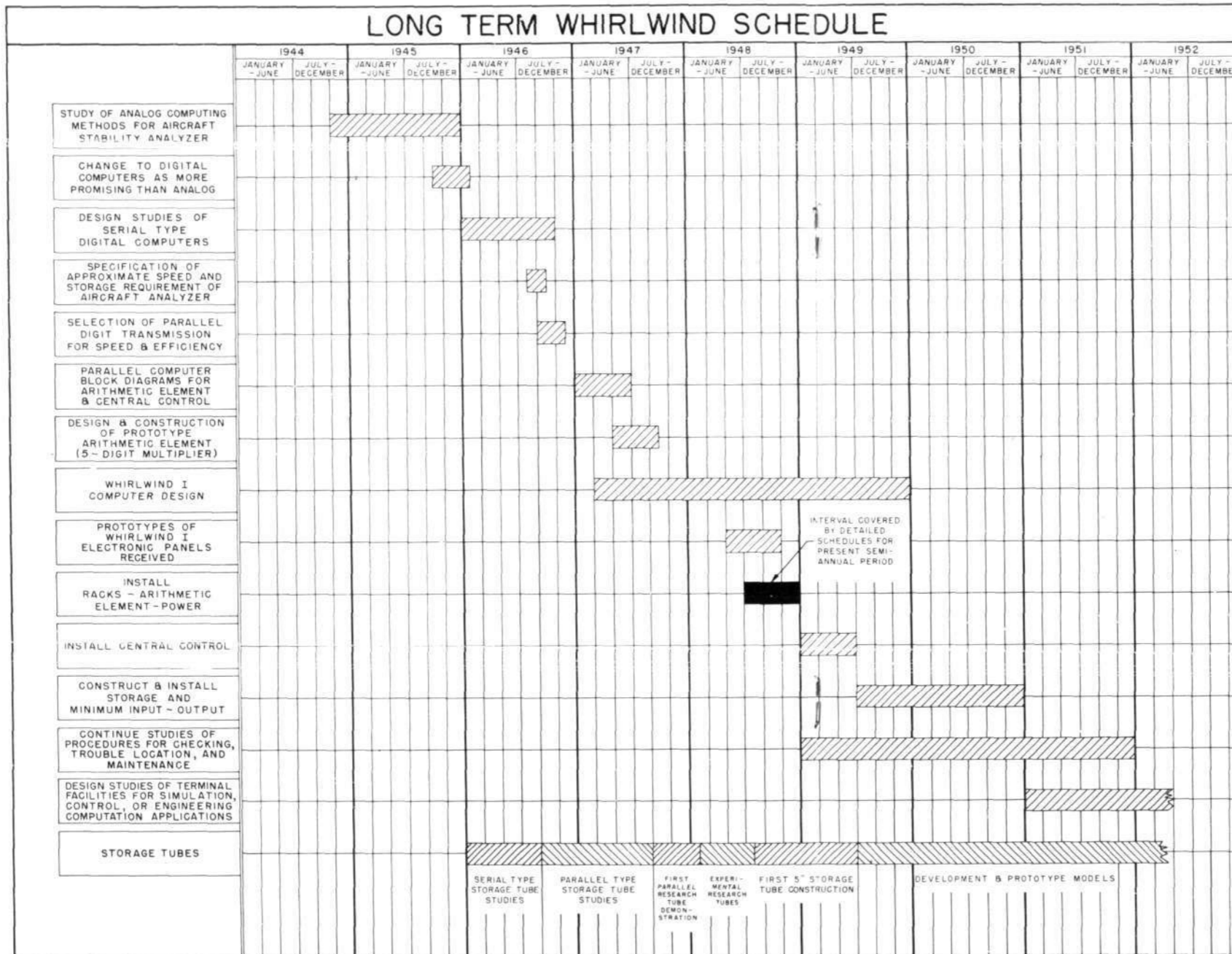
Date of latest posting.



Summary line. Shows overall status of the project.



Column showing whether M.I.T. or Sylvania will do major portion of the job.



Estimates assume Laboratory expenditures at the August 1948 rate. This time schedule is extended over previous estimates which were based on expanded laboratory facilities and subcontracting. Added staff and subcontracting could complete WWI at an earlier date and provide the applications studies, and the auxiliary equipment design and construction, required for useful full-scale operation.

STORAGE TUBES

General Status

As discussed in the July Summary Report, difficulties had been encountered in obtaining a 5-inch mosaic of beryllium squares. From a series of special evaporation tubes constructed in an endeavor to isolate the factors involved, a technique has been developed which furnishes good, well-defined beryllium mosaics. The method uses a small resistance-heated evaporation cup, shielded from the body of the tube by a mica shield mounted about 3/8 inch above the source. This shield prevents excessive heat from impinging on the mosaic surface and also prevents the evaporated beryllium molecules from reflecting from the glass walls of the evaporation tube back on to the target. With the final method it was possible to evaporate a well-defined shadow, using a wire mask 0.002 inch in diameter and 1/8 inch from the target surface.

This method of evaporation has resulted in a well-defined set of beryllium squares, but the thickness of the beryllium coating is not considered adequate. Therefore, work has been started on the development of a resistance-heated cup with a large supply of beryllium. An adequate design should result in an assembly which could be operated over a period of several hours of continuous evaporation, resulting in a thick mosaic with adequate definition. An evaporation tube having a resistance-heated crucible enclosed in heat-insulating material is being assembled.

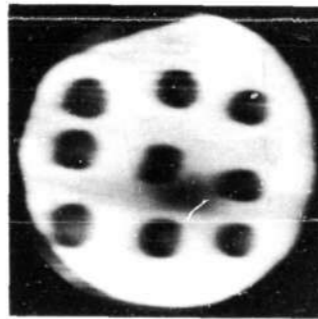
One of the thin 5-inch mosaics has been assembled into a tube and a second is being processed. Positive and negative spots of charge have been successfully stored on the surface of the first tube. An array of 121 spots has been maintained within a 2-x-2-inch area for a period of thirty minutes. However, this storage was obtained at an accelerating voltage of between five and seven hundred volts on the holding gun. It is expected that thicker mosaic surfaces will reduce this storage voltage.

Television Setup

The storage of binary digits by use of an electrostatic storage tube depends on the fact that a

given point on the storage surface is at one of two stable potentials. In testing storage tubes it is therefore important to know the potential distribution on the storage surface. One method of determining the potential is to "read out" the storage surface at a given point just as it would be read out in normal operation in the computer. However, this reading gives the potential at one point only. The television setup presents in picture form the potential distribution on the entire surface at every instant.

Basically the television setup is as follows: Two sweep generators (one for horizontal and one for vertical sweep) supply sweep voltages to both an ordinary television picture tube and to the high-velocity gun in a storage tube. The sweeps in the two tubes, being derived from one source, are always in synchronism. The high-velocity beam in the storage tube scans the storage surface. When it scans an area that is at the positive stable potential there is no output, but when it scans an area at the negative stable potential a positive output appears from the signal plate of the storage tube. The output from the signal plate is amplified by ordinary video amplifiers and is used to modulate the beam in the television picture tube. Bright areas on the television tube represent positive outputs from the signal plate and hence negative areas on the storage surface. Conversely, dark areas on the picture tube represent positive areas on the surface of the storage tube.



TELEVISION PICTURE-TUBE REPRESENTATION OF NINE POSITIVE SPOTS ON A NEGATIVE BACKGROUND ON THE 3/4-INCH TARGET OF AN EXPERIMENTAL ELECTROSTATIC STORAGE TUBE.

In this manner, an image is formed on the television tube which at every instant corresponds to the potential distribution on the storage surface. The accompanying photograph shows the portrayal on the television screen of nine positive spots on a negative background. The experimental storage tube has a surface coated with calcium tungstate, the fluorescence of this surface gives a visual indication of potential which can be compared with the picture-tube presentation.

Actually the sweep generators used are part of an ordinary television receiver adapted for the purposes of this setup. The sweep voltages are applied directly to the television picture tube, and through a resistance-capacitance voltage-divider network to the deflection plates of the storage tube. The output from the storage tube is amplified in an amplifier built for this purpose and in the two stages of video amplification in the television receiver, after which it modulates the picture tube. The picture thus obtained accurately portrays the potential distribution of the storage surface.

The television setup will be mounted in a rack and will be semi-portable for use in the storage tube laboratory. It will have three main functions:

1. To present a picture representing the surface potential distribution in tubes with beryllium or similar surfaces which do not fluoresce brightly and hence cannot be observed directly.
2. To study the spreading of spots on the storage surface with various electrode potentials.
3. To study the placement of spots on the surface.

GATE TUBE CHAIN PERFORMANCE

In electronic digital computers it is necessary to transmit information from one place to another in the computer. Transfer of information in WWI is accomplished by transmission of 0.1-microsecond pulses, each pulse representing a digit of the number to be transmitted. The routing of these pulses to the proper destination via a common bus system, as is done in WWI, requires an extensive and highly flexible switching system; the extreme operating speed of WWI necessitates the use of electronic switches, relays being too slow for the purpose. A fundamental unit of the electronic switching system

is the gate tube.

A gate tube is similar to a conventional pentode, with the exception that the suppressor grid is close-wound to permit independent control of plate current by both the control and suppressor grids. By application of the correct bias potential to one of the two controlling grids, the gate tube can be caused to transmit a pulse of plate current when a positive-going pulse of voltage is applied to the other grid. (In WWI, the control grid is pulsed and a bias voltage is applied to the suppressor grid.) Alternately, the tube can be made inoperative by proper biasing of the suppressor grid. Thus the suppressor-grid voltage can be used to control the presence or absence of a plate-current pulse when the control grid is pulsed.

Because of the characteristics of available tubes and components (the choice of which is seriously limited by the necessity of maintaining extremely high computer operating speeds) and because of the desirability of operating with control-grid bias fixed considerably beyond cutoff to provide a safe margin of discrimination against noise or spurious pulses such as transmission-line reflections, it has not been possible to realize a gain appreciably greater than unity in gate circuits. In certain sections of WWI a pulse must traverse serially as many as 16 gate tubes. Because of the near-unity gain of the gate circuits, concern has been expressed for the reliability of performance of these gate-tube chains.

Recent tests conducted on a chain of 15 gate tubes which closely simulates the high-speed-carry circuit of WWI indicate that with certain minor circuit revisions the operation of the gate-tube chains in WWI will be satisfactory. Improved performance has been realized by the use of increased plate-supply voltage, by simple circuit modifications, and by the use of improved-type 7AK7 gate tubes. The tests also indicate that pulse shape is not altered seriously by transmission through a large number of gate circuits, and that the original estimate of pulse-transmission time of 0.04 microsecond per stage for the basic gate circuit was sufficiently accurate.

In the course of investigation of certain types of gate-tube circuits, it has been observed that gate-

circuit output-pulse magnitude can be increased only a limited amount by driving the gate-tube control grid positive on input pulse peaks, with further increase in grid voltage actually resulting in a reduction of output-pulse magnitude. This effect, which can result in serious reduction of gate-circuit gain, has been traced to a characteristic of pentodes designed for gate-circuit applications. Minor circuit revisions or use of improved-type gate tubes minimize this effect.

MATHEMATICS

The main efforts of the mathematics group have been directed toward the investigation of numerical methods, suitable for the Whirlwind computer, for the solution of basic mathematical problems in applied analysis. The general end in view is to develop a method which when put into final code (a) is capable of solving as wide a class of problems as possible (such as the inversion of a non-singular matrix of order n , where n is any positive integer), (b) has a code consisting of as few orders as possible, (c) takes up the minimum amount of machine time, (d) requires the minimum amount of machine storage, and (e) is mathematically reliable, that is, provides sufficient control on the accumulation of truncation and round-off error. Usually these various objectives tend to conflict with each other, and the problem is therefore to attain an optimum compromise.

Simultaneous Linear Algebraic Equations

A complete code, except for input and output orders, has been drawn up for the solution of simultaneous linear algebraic equations by elimination. The code is designed to handle an arbitrary number of equations. To solve any particular given system it will be necessary to insert into specified positions in storage only two parameters, the storage register number where the first coefficient is stored, and n , the number of equations. In addition to $(n^2 + 2n)$ storage registers for the coefficients in the equations and for storing the unknowns, the code requires 250 registers for orders and auxiliary data. Thus for fewer than 15 equations the "data" requires fewer storage registers than the program, while for more than 15 equations the

reverse holds. The coding technique, which makes the same control program applicable to any number of equations, is economical of storage space for any number of equations above 3. The code includes scale-factor control to keep all numbers in the computation within the machine range, -1 to +1. About 35% of the control program is used for this purpose. The estimated machine operating time, exclusive of input and output, is 0.1 second, 0.8 second, and 3.0 seconds for systems of 5, 10, and 15 equations respectively. At least for Whirlwind I, the code should be considered as intended for fewer than 15 equations, since for larger numbers the round-off errors will probably be excessive, in which case a so-called "iteration" or "successive-approximation" scheme would be used.

An investigation of iteration methods for the solution of systems of linear algebraic equations has been completed but no coding has yet been done. Given a system of equations

$$\sum_{j=1}^n A_{ij}x_j = b_i \quad (i=1,2,\dots,n)$$

we say we are using an iteration method, if, given an initial "guess" at the solution, $x_i^{(0)}$ ($i=1,2,\dots,n$), we successively modify this guess at each iteration until the result is sufficiently close to the exact solution. If it is possible to modify the guess in such a way that the result is actually improving, then the scheme is said to "converge". The major advantage of these successive-approximation methods is that they permit a much stronger hold on round-off error than elimination methods. Theoretical study, together with numerical experimentation, shows that the Seidel method is probably the most suitable one because (a) convergence of the iterations to the correct solution is easily assured, (b) convergence is rapid, (c) a way of instructing the machine when to stop iterating is available, and (d) coding is simple because the process is highly repetitive. Iteration methods in general, and the Seidel method in particular, are suitable for solving systems of order higher than could fit into the electrostatic storage all at once, since the various equations of the system are handled individually and need therefore be introduced into the high-speed storage only one at a time.

Integral Equations

The study of iteration procedures for linear systems was carried on using operational matrix notation, and this has proved useful in the investigation of the numerical solution of integral equations. Solution of the Fredholm equation

$$f(x) = g(x) + \lambda \int_a^b K(x,y) f(y) dy$$

presents no difficulties. A survey indicates that an iteration scheme such as Newton's for obtaining a solving kernel $R(x,y)$ such that

$$f(x) = g(x) + \lambda \int_a^b R(x,y) g(y) dy$$

would be best. A reduction to linear algebraic equations by approximate quadrature is also possible. The equation of the first kind

$$g(x) = \int_a^b K(x,y) f(y) dy$$

presents difficulty because it may have one, none, or many solutions of a certain functional class. In special cases iterative methods may be employed to advantage, and a back-substitution method will yield the result. An approximate solution, however, can usually be found by a least-squares procedure. For kernels of a special type, Fourier integral treatment provides an adequate numerical solution.

Differential Equations

Investigations supplementing those of the Runge-Kutta method for the solution of ordinary differential equations with given initial conditions have been undertaken. In the case of second-order equations the Nystrom variation of the Runge-Kutta method effects a considerable saving of machine time at the expense of only a slight increase in code length. When the first derivative is absent, this saving amounts to more than 25%. Since second-order equations occur so frequently in mathematical physics, a special method for solving them may be justifiable.

Representation of Empirical Functions

The problem of representing empirical functions of one or more variables by analytic approximations has also been studied. Smooth monotonic functions of a single variable can be fitted in a least-squares sense by orthogonal polynomials of the second or third degree to an accuracy of three

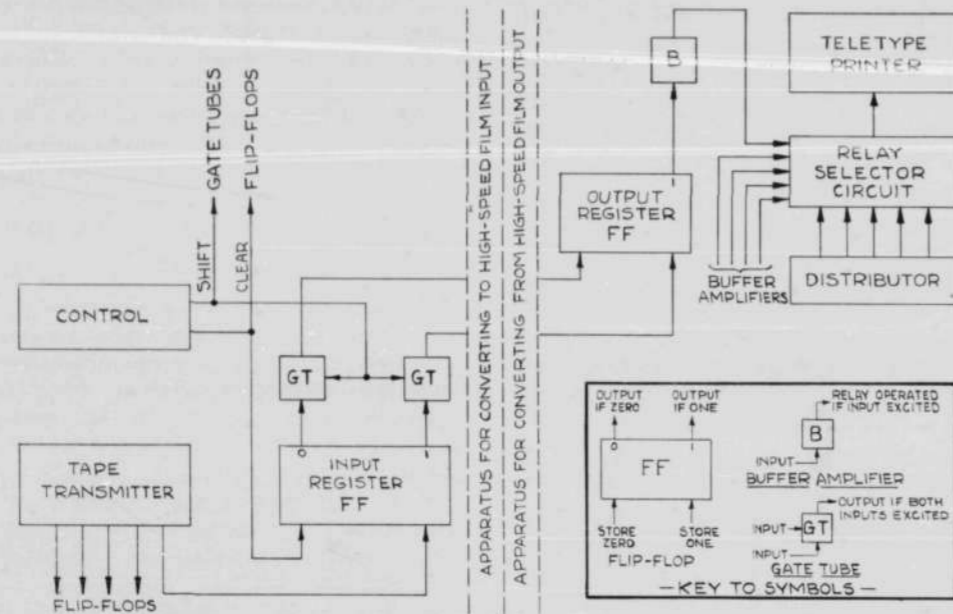
decimal places. If the approximating function must give a close representation for not only the function itself but also its first derivative, as is sometimes necessary for instance in simulation problems, the least-squares property of the fit must be dispensed with in the case of non-monotonic functions, but good results can nevertheless be obtained. Functions of several variables can be represented in a least-squares sense by a polynomial in the variables involved that gives least-squares fits to each of the variables individually.

TELETYPE INPUT-OUTPUT DEMONSTRATOR

A teletype input-output demonstrator has been built that automatically reads information into a flip-flop register from a perforated tape and reads information out of a flip-flop register for tabulation on a standard Model 15 teletype printer. The information is assumed to be in the standard teletype five-unit code. The reading-in function (368 operations per minute) is desirable in order that the same information can be recorded on a photographic film for later high-speed input to the computer. The reading-out function will be associated with the equipment which converts an output film to printed page copy.

The simplified block diagram indicates the basic elements of the teletype input-output demonstrator. (For conciseness, the diagram shows only one each of the components that are repeated for each of the five digits of the teletype code.) The tape transmitter section of a standard Model 14 transmitter-distributor is employed to read five-unit teletype code combinations from a perforated paper tape into an input register consisting of five flip-flops. The control circuits perform the functions of shifting the teletype code combinations held in this electronic register through gate tubes to other registers, and clearing the input register before the next reading-in operation takes place.

Through buffer amplifiers, the five flip-flops in the output register control the energizing of relays in the relay selector circuit. Teletype code combinations held in the output register are thus stored momentarily in the settings of these relays. The distributor of a standard Model 14 transmitter-dis-



TELETYPE INPUT-OUTPUT DEMONSTRATOR

tributor is used to read these relay settings and transmit a serial seven-unit teletype signal to the receiving printer. The necessary synchronizing start and stop signals for the printer are automatically produced during each revolution of the distributor brush. All of the machine functions performed normally by a teletype printer (spacing, carriage return, line feed, and shifting) are ordered by the code combinations supplied to the output register. One model of the demonstrator that was constructed provided for automatic machine functions that are sometimes desirable.

The teletype demonstrator has provided valuable information for the final design of intermediate low-speed input and output devices: the operational characteristics of the teletype equipment itself have been established, and suitable electronic and relay circuits have been designed and tested.

VISITS

Visitors to the Laboratory

During August the Laboratory had among its visitors the following:

Dr. Alan T. Waterman, of the Office of Naval Research.

Lt. Col. J. H. Kusner (USAF), of the Military Requirements Division of the Munitions Board, who devoted two days to a study of project work.

S. N. Alexander, of the National Bureau of Standards.

Lawrence C. Mansur and Chester Malik of the Electronic Research Laboratory (USAF) to discuss storage tube design and construction.

Commdr. Norman T. Ball (USNR) and twelve other student Naval officers of the MIT Radar School.

Capt. U. P. Cogswell (USN), of the Air Navigation Development Board, to discuss air traffic control.

T. M. Berry, W. C. Hahn, G. W. Hobbs, B. R. Lester, and D. R. Rodgers, all of General Electric,

to discuss problems of computer design for guided missile control.

R. T. Gabler, of North American Aviation Company.

Dr. I. J. Gabelman, of Watson Laboratories, and Dr. R. F. Nicholson, of the Electronic Research Laboratory, to discuss air traffic control.

Dr. David M. Myers, of the Council for Scientific and Industrial Research, Australia.

George E. Gourrich and William L. Martin of the National Bureau of Standards.

Visits by Project Staff Members

Mr. J. W. Forrester, Supervisor of the Project, and Mr. R. R. Everett attended the Modern Calculating Machinery and Numerical Methods Symposium at the University of California, Los

Angeles, July 29, 30, and 31. Mr. Forrester delivered a talk in which he described characteristics of the Whirlwind computer and discussed applications of high-speed digital computing machines. He pointed out that the perfection of these machines and the development of techniques for their application and use constitute a task of much greater magnitude than has often been supposed, and that its achievement will require large expenditures of time and money. Copies of Mr. Forrester's talk, published as Report R-142, may be obtained from the Project.

During their trip Messrs. Forrester and Everett visited several Government and commercial laboratories to discuss possible computer applications.

APPENDIX
REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were among those issued during August:

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
SR-9	Summary Report No. 9	16	-	6-48	
R-139	Vacuum-Tube Life	43	35	6- 1-48	D. R. Brown M. H. Hayes J. J. O'Brien
R-140	Gas Discharge Gaps for Data Storage in Electronic Computers (Abstract in E-140)	114	43	7-21-48	R. F. Markel
R-141	Rectifier Networks for Multi-Position Switching	5	9	8-31-48	D. R. Brown N. Rochester
E-126	Scope Synchronizer	3	1	7-21-48	R. L. Best
E-131	Testing of B-Register/In-Out Register, Digit Panel	9	3	6-29-48	R. H. Gould
E-136	Testing of Bus Driver Panel Prototype	4	7	7-29-48	R. H. Gould
E-137	Performance of Chains of Gate Tubes	7	9	8- 5-48	J. M. Hunt
E-138	Transient Analysis of Pulse Transformer Load	9	10	8-13-48	D. R. Brown
E-139	7AK7 Characteristics	7	7	8-25-48	J. M. Hunt A. K. Susskind
M-465	Proposal for Restorer-Pulse Distribution	3	1	7- 7-48	G. G. Hoberg
M-478	Circuit Schematic Component Serial Numbers	1	-	6-15-48	A. M. Falcione
M-547	Design of RT34 Holding Gun	5	1	7-21-48	H. Klemperer
M-549	Comment on the Two-Register Method	4	-	7-22-48	C. W. Adams
M-551	Visit to Power Equipment Company, July 2 and 12, 1948	3	-	7-22-48	H. R. Boyd
M-554	Eastman Conference of July 13, 1948	4	-	7-27-48	H. R. Boyd
M-555	Demonstration of the Transistor at Bell Telephone Laboratories	2	-	7-27-48	E. S. Rich
M-556	Electronics Group Meetings, June 25, July 2, 9, and 16	2	-	7-27-48	J. J. O'Brien
M-558	Installation of Permanent Fixtures for WWI	2	-	7-29-48	C. W. Watt
M-563	Holding Gun Stability Tests on ST32 (June 3 to July 9)	8	12	7-29-48	J. S. Rochefort
M-564-1	Rack Modification for Power Bay	2	-	8- 4-48	R. E. Hunt
M-566	Reduction of Trigger Tube Input Admittance; Parasitic Oscillations in Trigger Tubes	1	-	8- 5-48	J. M. Hunt

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
M-567	Bi-Weekly Report, Part I, August 6, 1948	13	-	8- 6-48	
M-568	Bi-Weekly Report, Part II, August 6, 1948	17	-	8- 6-48	
M-572	Approval of Rack Fuse and Terminal Strips	1	-	8- 9-48	H. S. Lee
M-574	Review of Power Requirements for the -15 and -30 Volt Supplies WWI	1	-	8-10-48	H. S. Lee
M-575	Recent Studies of Evaporation Techniques	4	-	8- 6-48	R. Shaw
M-576	Resistance Measurements on Beryllium-Evaporated Targets	2	3	8-12-48	M. Florencourt
M-580	E-136, E-131 and E-137, Comments	2	-	8-19-48	J. W. Forrester
M-581	Location of D. C. Filter Panel	1	1	8-20-48	H. S. Lee
M-584	Progress Report: Trouble Location in a Large Scale Electronic Digital Computer	2	1	8-10-48	G. C. Sumner
M-585	Bi-Weekly Report, Part I, August 20, 1948	14	-	8-20-48	
M-586	Bi-Weekly Report, Part II, August 20, 1948	17	-	8-20-48	
M-588	The Divide Control	3	1	8-23-48	N. L. Daggett
M-589	Fixed Voltage Switching Panels, Production Testing	1	-	8-24-48	C. W. Watt
M-590	Control Switch and Storage Switch Drawing	1	-	8-24-48	J. A. O'Brien
M-591	Restorer Pulse Generator Change	1	-	8-24-48	J. A. O'Brien
M-592	Sylvania-MIT Meeting, August 25, 1948	2	-	8-26-48	C. W. Watt
M-593	Progress Report: Trouble Location in a Large Scale Electronic Digital Computer	2	-	8-20-48	G. C. Sumner
M-594	The Multiplier Error Detector	2	1	8-26-48	N. L. Daggett
M-595	Register Driver Type I Layout Approval	1	-	8-27-48	N. H. Taylor
M-596	Critical Temperature of Condensation of Atomic Metallic Vapors	5	1	8-30-48	M. Daniloff
M-598	Circuit Research, Present and Future Work	5	-	8-27-48	D. R. Brown
M-600	Mounting Holes for D. C. Filter Panel Bracket	1	1	9- 1-48	H. S. Lee
M-601	Revision of Control Switch Block Schematic, T60CS00-4	1	-	9- 2-48	J. A. O'Brien
C-58	Meetings of the Mathematics Group: The solution of Systems of Linear Algebraic Equations by Successive Approximation	4	-	7-29-48 8- 3-48 8- 6-48	E. Reich

<u>No.</u>	<u>Title</u>	<u>No. of Pages</u>	<u>No. of Drwgs.</u>	<u>Date</u>	<u>Author</u>
<u>Translations</u>					
142	The Pulse Transformer (Department of Commerce, Publication Board, Publica- tion No. 74821) by Dr. Grasl	57	44	3-7-48	J. M. Salzer

Tables

The following tables have been computed and reproduced by hectograph:

1. Powers of 2 from -20 to 51 in unit steps.
2. Binary equivalents, 1 to 1,000,000.
3. Binary equivalents, 0.00001 to 1.

Copies of these tables will be sent to those who have need for them.