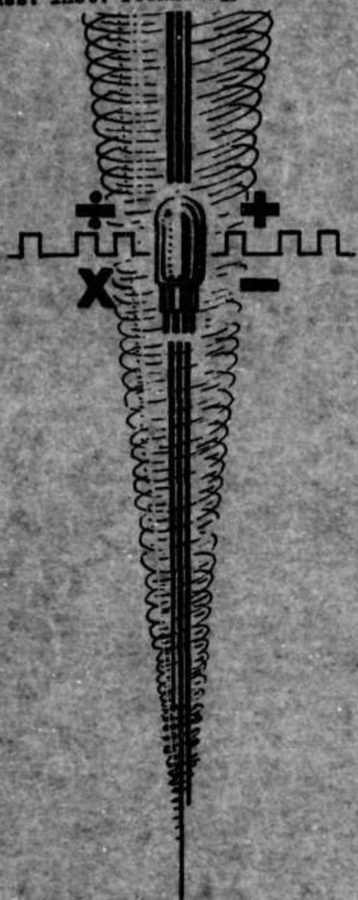
SL-SR-8

PROJECT WHIRLWIND

Contract N5ori60



SUMMARY REPORT NO. 8

MAY, 1948

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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DEPARTMENT OF THE NAVY
OFFICE OF NAVAL RESEARCH

SPECIAL DEVICES CENTER

[redacted]

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 8

MAY 1948

Submitted to the
SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
under Contract N5ori60
Project NR-720-003

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts
Project DIC 6345

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

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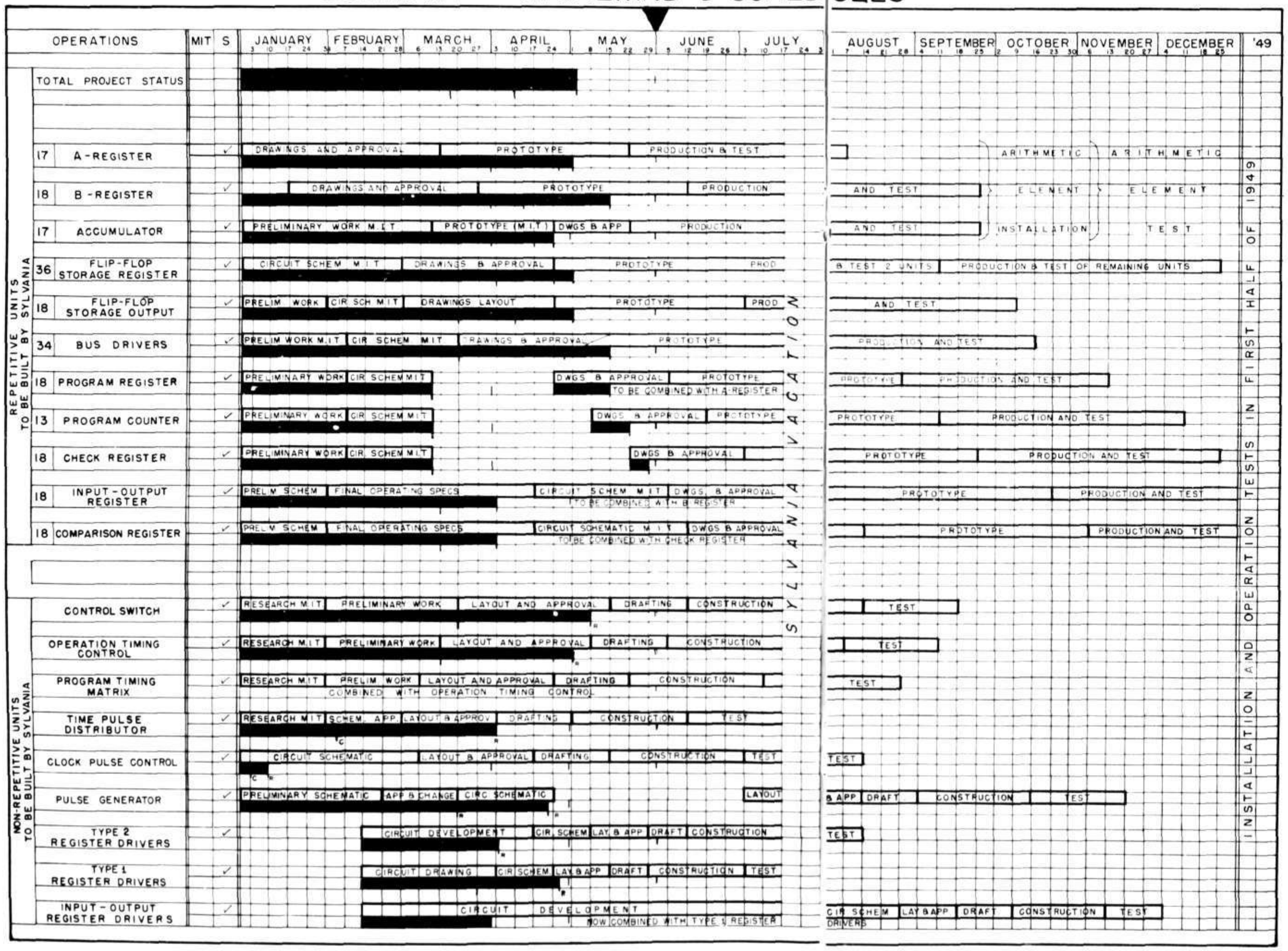
SUMMARY - WHIRLWIND I SCHEDULES



LEGEND

JANUARY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in January 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

Diagonal line indicates overlapping of two operations.

MIT | S

Column showing whether M.I.T. or Sylvania will do major portion of the job.

NOTES

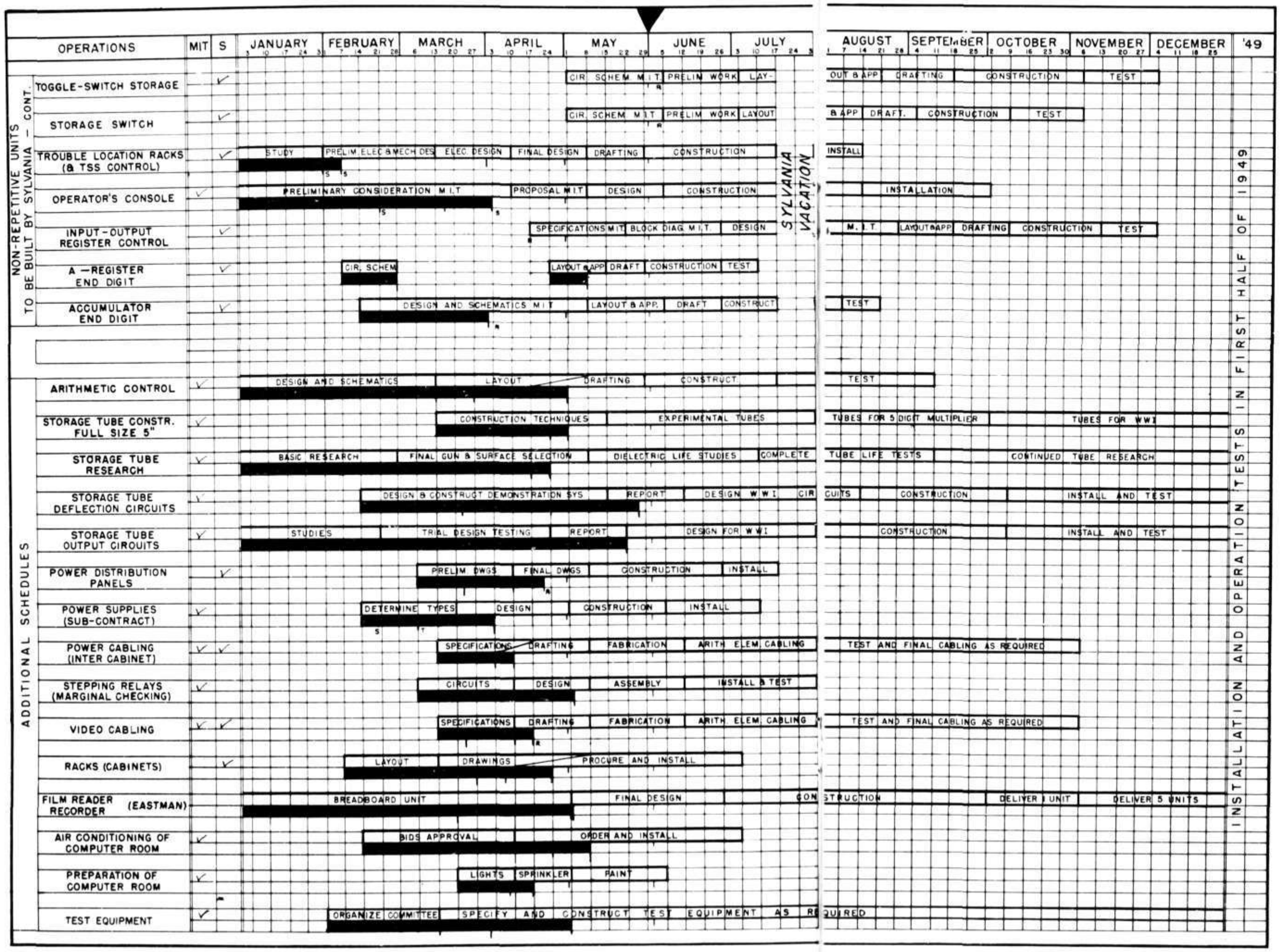
C Changes in specifications have delayed this item.

S Studies and specifications still incomplete, due principally to lack of staff time.

R Revised schedule does not call for same completion date as originally planned.

T Temporary arrangements can be made to meet required schedule.

SUMMARY - WHIRLWIND I SCHEDULES CONT.



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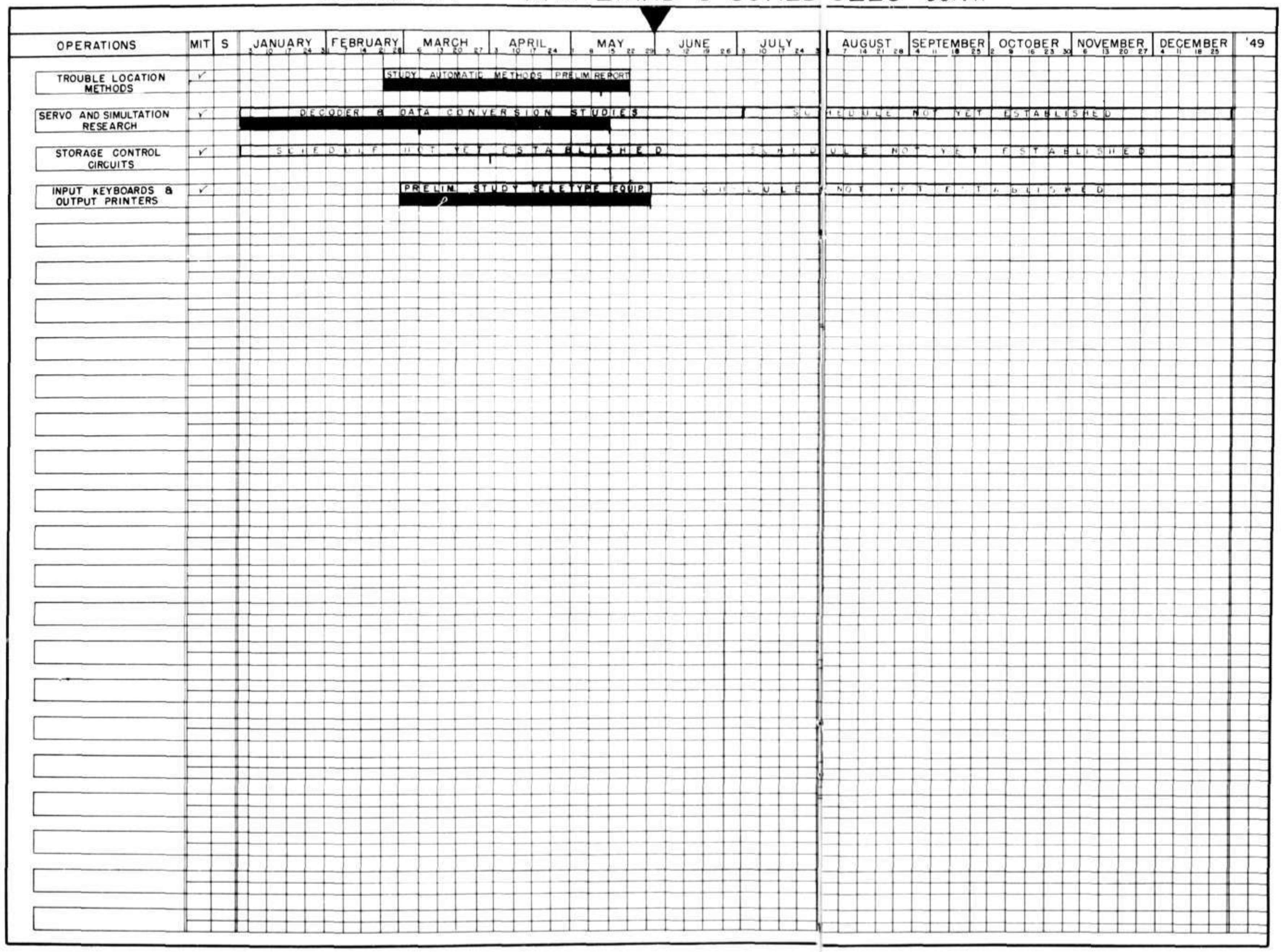

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GENERAL STATUS

As shown in the summary chart, Whirlwind I progress is running about four weeks behind the schedule set up at the beginning of the year. Construction time will be materially reduced by the recently arranged interchangeability of equipment between three pairs of registers, as reported in the following article; the schedules do not reflect the results of this change, because additional time is required for analysis.

The room in which the WWI computer will be housed is being made ready for the installation of cabinets and equipment. A short article in this Report describes the provisions for various facilities in the computer room.

Additional effort is being put into the storage tube program, with several additional staff members assigned to this work.

INTERCHANGEABILITY OF REGISTERS

The block diagrams of Whirlwind I call for 9 registers of 16 digits each. Original plans were to design 9 panels and build 16 of each plus appropriate spare units. It has recently become apparent that a sufficient similarity exists between certain of these registers to permit the use of interchangeable panels in 3 pairs of registers. This will require rather minor changes in 3 of the 9 panels, which will result in a slight production delay; but 3 designs which had not progressed beyond very preliminary stages can be abandoned. The total engineering and production time and cost is materially reduced by this identity of A-register and program register equipment, B-register and in-out register equipment, and check register and comparison register equipment. In addition to the increase in engineering and production efficiency, a slightly smaller total number of panels will be needed on account of the interchangeability of spare units.

POWER DISTRIBUTION FOR TROUBLE LOCATION BY VIDEO AND D-C METHODS

Summary Report 6 described in general terms the system of trouble location by check and trouble-location problems that is proposed for WWI, and discussed the system of power distribution that when used with these video methods will enable marginal operation of components and circuits to be detected before they cause trouble in actual computation.

The whole power distribution system, including marginal checking equipment, fuses, voltage-variation panels, indicators, *etc.*, is idealized in the typical circuit shown in the block diagram on page 10. This system connects the digit columns by pairs, the voltages to each pair being supplied through one set of voltage-variation panels. Fourteen lines are supplied to each digit column. All are switched by relays, and a variable voltage generator may be inserted in series with any one of 11 of the 14. Since there are 16 digit columns, 88 voltage-variation circuits are required.

Analysis of the general problem of trouble location shows that there are two ways by which a fault may be located, each of which has its own application. One method merely indicates and locates the presence of a short anywhere in the circuits. The other, using groups of trouble-location problems, utilizes video techniques to isolate a fault. This method is especially useful if the trouble is intermittent or is due to deterioration of tubes or other components, and is used both in locating a fault that occurs during regular computation, and in marginal checking.

If the trouble is one that produces a real short circuit at any place in the computer, it seems logical to locate that trouble directly. Thus, since a short circuit in a load will usually blow the fuse feeding the load, each circuit carrying power to a panel in the racks is protected by a fuse of the Western Electric Indicator Alarm type. When a fuse blows, it switches the supply voltage for its line to a back contact which in turn activates one of a number of relays. These relays have several functions. First, they turn off a green "on" light at the operator's console, and switch on a red "trouble" light. Second, they light a red "column" light, and a red "row" light, thus indicating in which rack the short has occurred. Third, they take the power off the relays in the voltage-variation panels which feed the affected column of racks. When a short occurs the operator merely goes to the indicated rack, and the fuse that has blown is evident because of the indicator flag that springs up when the fuse wire breaks. The power now being off, the fault can be isolated by d-c methods and the fuse replaced.

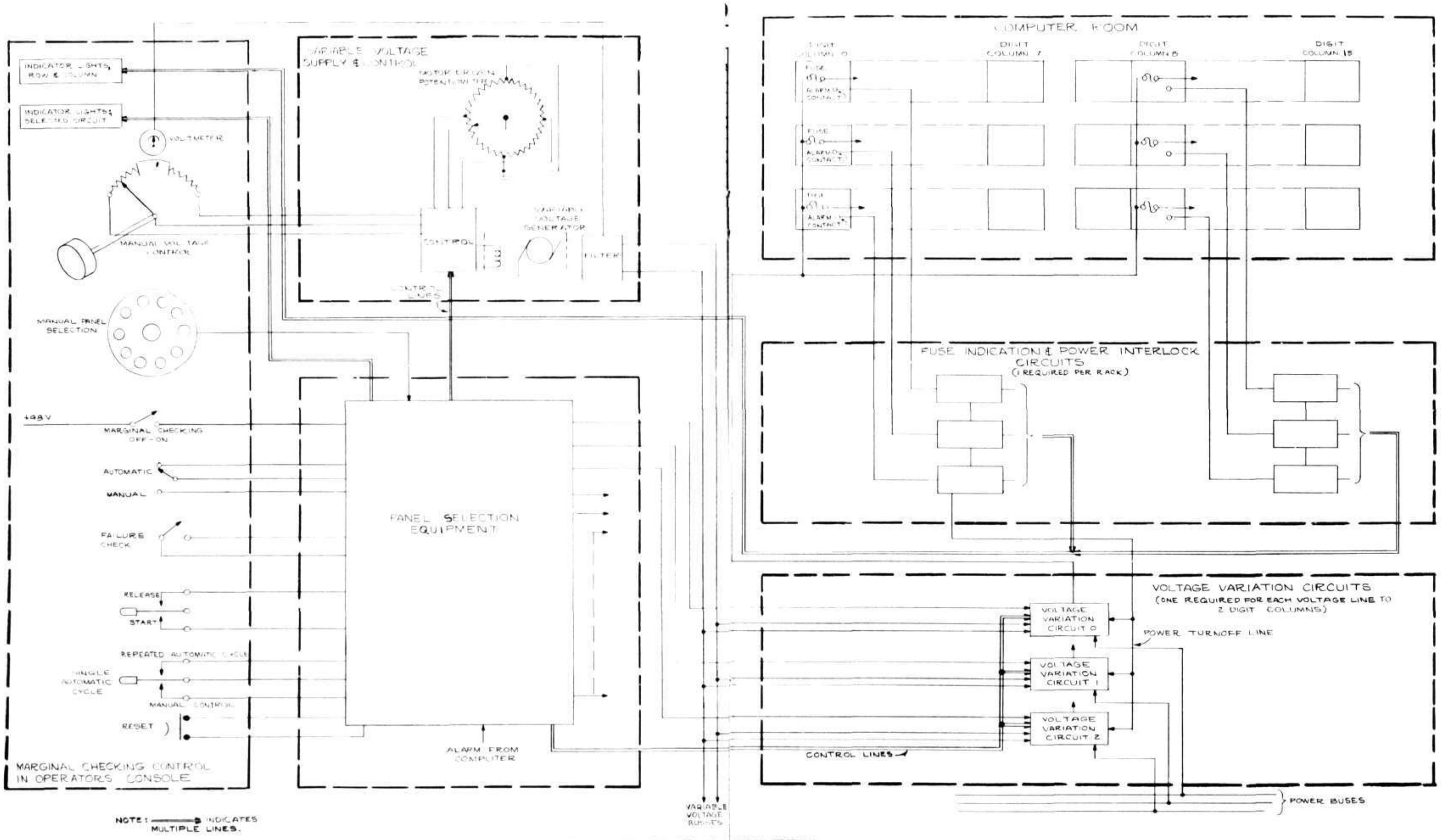
The video checking method locates more subtle failures, such as intermittent connections or deterioration of tubes or components. As used with the marginal checking equipment, it helps reduce operational failures, for by these techniques troubles that might occur during the solution of a problem can be anticipated and their causes removed before real operational time is lost. Variation of tube electrode voltages in a predetermined way (accomplished by the marginal checking equipment) while the computer is solving standard test problems forces components whose operation would normally be marginal to fail steadily; these failures can then be located and repaired.

A typical marginal checking sequence might be as follows:

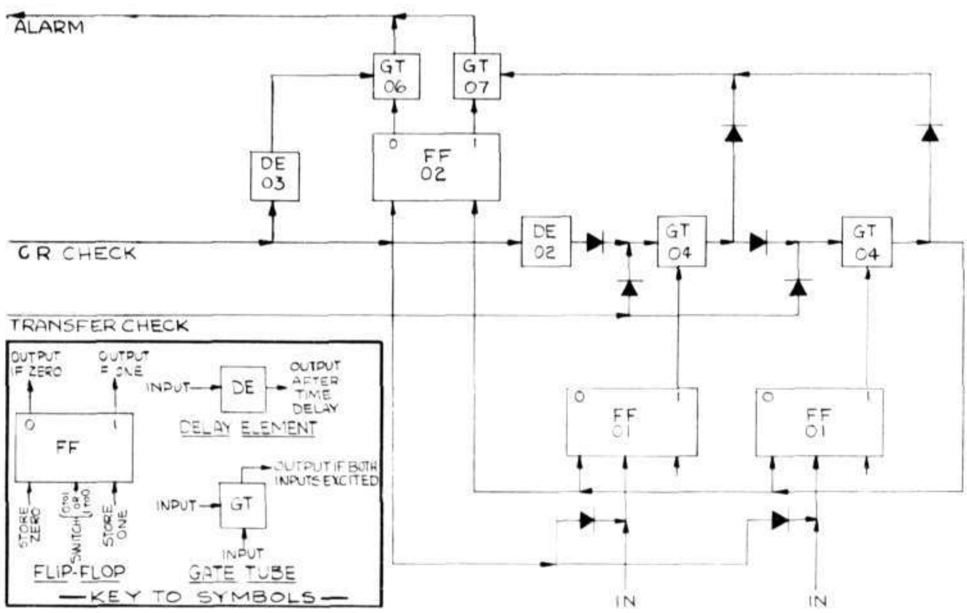
Before the computer is set up for a regular problem it will be checked to see that everything is in working order. Accordingly, the marginal checking "on-off" switch on the console is turned on. (See the block diagram.) A "manual-automatic" switch is placed on "automatic", and the "start" key depressed. The panel selection equipment is in position 0, and voltage variation circuit 0 is activated. When the relays in this circuit have operated, the variable voltage generator has been put in series with the power line fed by V. V. circuit 0, and proceeds to vary the voltage on that line in a cycle above and below its regular value. At the same time the computer is repeatedly solving a short check problem designed to operate all the circuits at least once. The solution time of this problem is very short compared to the period of the variable voltage cycle, so that each solution is completed at nearly a constant voltage. At some point in the cycle, a marginal tube or component may produce an error in the result. If this occurs, the checking equipment of the computer detects it, stops the clock supplying pulses to the computer, and applies a brake to the motor-driven potentiometer which varies the field of the variable voltage generator. The voltage applied to the circuit thus remains close to the value it had when the error occurred, and can be read from a meter. The operator now inserts the "trouble-location" problem groups in the computer, and turns on a "failure-check" switch. This first brings the voltage on the circuit being varied back to its normal value. The operator now starts the computer again and by means of a manual voltage variation control varies the voltage until the failure again occurs. At this point the trouble-location problems will cause an indication to be given on a bank of lights, which will be a coded indication of where the failure occurred. Since the voltage is being varied on only 2 digit columns, since in general that voltage is used for only one or two purposes in the circuits, and since the trouble-location problems test each register separately, failures can be located to within one or two tubes in a register.

When the trouble has been located and cleared - whether by replacing a tube or a whole panel - the checking sequence is continued by turning the "failure check" switch off. The selection equipment then selects the next circuit to be checked, checks it, and steps on, circuit by circuit, either until another failure occurs or until all have been checked. When a failure occurs and proves to be intermittent, the circuit may be checked repeatedly by putting the variable voltage generator on "repeated automatic cycle". Selection of any one circuit for manual or repeated automatic cycle may be made without going through the complete automatic panel selection sequence. Selection is done from the console by a telephone dial, the number of the panel desired being dialed.

Considerable progress has been made in transforming these concepts into actual equipment. The whole system has been clarified and integrated, schematic diagrams have been drawn for all parts, layout of the various relay panels required are over half finished, and fabrication of power cables for the computer racks has begun.



WWI POWER DISTRIBUTION SYSTEM
SIMPLIFIED REPRESENTATION SHOWING
ONLY TYPICAL CIRCUITS



CHECK REGISTER CHECKING

CHECK REGISTER CHECKING

Simple failures in digital computers can entirely destroy the correct answers to problems, and such errors might never be detected unless the problem is re-done by hand or by another machine, or unless the computer has its own trouble-location system.

In WWI, in addition to trouble-location methods which use special problems (see the March Report), a built-in "transfer check" system is used which will reduce the number of errors which can occur without detection. This system checks the bus-transfer of all 16 digits from one place to another, and is used in nearly all cases where bus-transfers occur. A register known as the "check register" is used for this check.

The check register is a flip-flop register which operates by having the transferred number read into it twice (from the transmitting and from the receiving registers) in such a way as to clear the register if the same number is received both times. Gate tubes are connected to the flip-flops of the check register and are pulsed after the second read-in. If any flip-flop of the check register now holds a 1 (signifying an erroneous transfer) the pulse will get through the gate tube that is connected to that flip-flop and will ring an alarm.

It is possible for the check-register flip-flop itself, or its gate tube, to be inoperative so that no alarm will ring. For this reason, it is also necessary to check the check register. Recently added equipment does this once every "order" by changing the check register to all 1's and making sure that all gate tubes will pass a pulse.

The very much simplified block diagram shows how this is done. Flip-flops **FF01** and gate tubes **GT04** represent the check register. Flip-flop **FF02** is normally set on 1. The normal transfer check pulses each **GT04** separately, and if any **FF01** holds a 1, a pulse will pass through its **GT04** and through **GT07**, and ring an alarm. The check-register check ("**CR** check") pulse goes to **DE02** and **DE03**, clears **FF02**, and complements all **FF01**'s so that if they all were previously on 0, they all will now be on 1. The pulse emerging from **DE02** will then run through all **GT04**'s in series, will not pass through **GT07** (since FF02 is on 0), but will clear all FF01's and will set FF02 to 1. If any FF01 or GT04 is not operating correctly, the pulse will not arrive to set FF02 to 1, and the pulse from DE03 will pass through GT06 and will ring an alarm.

This new checking equipment checks itself and will give an alarm if it fails to operate. Simultaneous failure of all parts of the new circuit, however, will not produce an alarm. But such a failure is unlikely to occur and will be discovered by daily (or other periodic) checks if it should occur.

PREPARATION OF COMPUTER ROOM

The forthcoming installation of computer equipment has necessitated certain special preparations of the computer room. Engineering and preliminary layouts of the 60-kw air conditioning system have been completed (see Summary Report No. 4), and the order for the penthouse to house this equipment has been placed. Shop work has been completed for conversion of the sprinkler system to an air-filled system, in order to reduce the hazard of wetting the computer equipment.

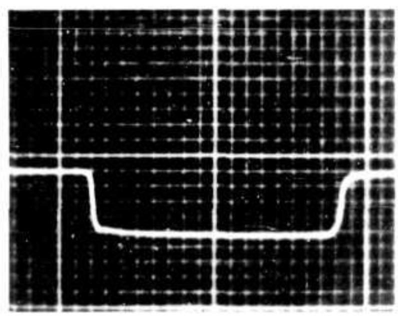
Lighting will be provided by both overhead fluorescent fixtures already installed and cabinet lights which will be mounted on the wire raceways over the aisles.

Five wire raceways 4 inches square have been installed between the computer room and the power room to bring two a-c circuits and many d-c power leads up to the power panel cabinets. D-c supplies in the computer room will include, in addition to power for the computer, connections to the central laboratory power supply available at convenient points for the operation of test equipment and for running sections of the computer for special purposes.

MAGNETIC RECORDING

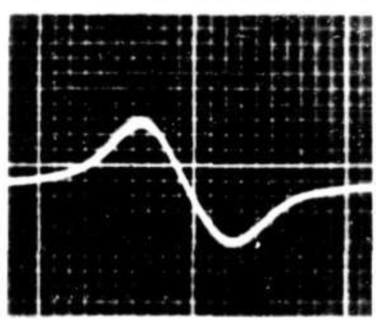
Magnetic material may be used as a storage medium in electronic computers for those memory functions in which a comparatively long access time is permissible and in which extremely high reading and writing speeds are not required. An investigation is being conducted to determine possible applications of magnetic recording to the input and output devices of the Whirlwind computers.

Since it is desirable that the information be recorded in the form of coded binary numbers, a study has been made of some of the principles involved in recording pulse signals which may be used to represent such numbers. A Vicalloy tape was used as the recording medium, and the magnetic heads were placed in contact with the tape. In the experimental work that has been performed, signals were recorded for both zeros and ones and these digits were distinguished by the polarizations of the magnetized sections of the tape. The input signals used were such as to produce approximately rectangular pulses of current through the recording-head winding, as shown in the oscillogram of Fig. 1.



HORIZONTAL SCALE - 0.48 μs/div
VERTICAL SCALE - 11 ma/div

FIG. 1 CURRENT PULSE THROUGH RECORDING HEAD WINDING

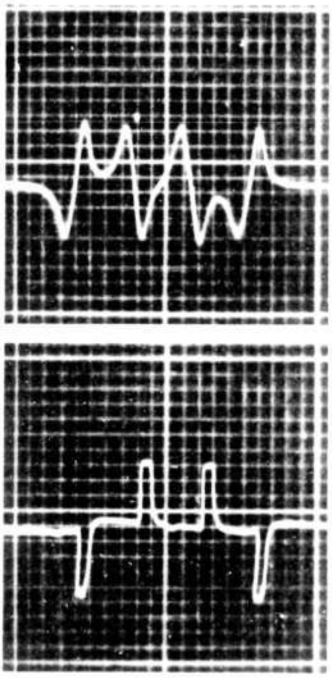


HORIZONTAL SCALE - 2.2 μs/div
VERTICAL SCALE - 98 mv/div
TAPE SPEED - 20ft/sec

FIG. 2 VOLTAGE GENERATED IN PLAYBACK HEAD WINDING

A typical playback pulse, then, exhibits both a positive and a negative voltage swing and resembles one cycle of a sinusoidal voltage; see Fig. 2. It was found that an optimum input-pulse amplitude and length exist that will produce the shortest output-pulse length for a given output-pulse amplitude. These input values were used in determining the maximum recording densities or numbers of pulses per unit length of tape that can be obtained.

In order that the output signals be in a form more suitable for driving additional pulse equipment, a reshaping circuit was designed which will convert the double-swing output signals into narrow rectangular pulses of the proper polarity; see Fig. 3. With this circuit, the maximum recording densities were measured with the Vicalloy tape driven at a speed of 20 ft/sec. The values obtained



HORIZONTAL SCALE - 9.7 µs/div
VERTICAL SCALE UPPER - 98 mv/div
LOWER - 7 v/div

FIG. 3 ABOVE: VOLTAGE PULSES (POSITIVE AND NEGATIVE) FROM PLAYBACK HEAD
BELOW: RESHAPED PULSES

depend on the playback-pulse amplitude selected, and range from 90 pulses per inch for signal-to-noise ratio of about 110 to 180 pulses per inch for a signal-to-noise ratio of 20. These signal-to-noise ratios are those between peak playback-pulse amplitude and the peak amplitude of the noise obtained from a demagnetized tape.

Since input and output devices require that the location of recorded information be known, a means of positioning the magnetic medium is necessary. Some work has been done on the development of a reading head in which an output corresponding to a recorded signal is produced when the tape is stationary or is moving at a slow speed. The head is designed so that the presence of a magnetized portion of the recording medium over the head will produce a change in the head inductance. This change of inductance is then detected by an a-c bridge circuit to give a usable output signal. Since the change of inductance is obtained by partial saturation of a narrow constriction in the core of the head, it is possible to increase the sensitivity of the head by introducing a d-c component of flux in the core so that the head operates under conditions which give the maximum percentage change of inductance for a small change in the d-c flux component. This bias flux also makes it possible to distinguish the polarization of the magnetized portions of the recording medium by sensing the relative phase of the unbalance-voltage from the bridge.

In a static reading head that has been built, about a 10 percent change of inductance was produced when a magnetized section of Vicalloy tape was brought over the head. With the bridge circuit used, this corresponds to an unbalance-voltage that is about 30 db above that at the null. These results indicate that such a head might be used to detect marker signals recorded in a separate channel on a tape or drum and to furnish an output to control a servo-positioning motor. It might also be used for reading recorded information at the slow speeds required for operating an output printer.

Further experimentation is necessary to determine the best method of driving and positioning the recording medium and to determine what operating speed is most practical. From the tests that have been conducted, it is evident that the heads must be spaced away from the surface of the recording medium to eliminate wear if speeds greater than a few feet per second are used. Therefore, an investigation of recording under such conditions is also necessary.

VISITORS

During May the Laboratory was visited by several groups interested in project status and in applications of digital computers to their fields of interest. These included Cmdr. Morgan, Lt. Comdr. Rowley, H. C. Calpine, and W. A. Wykeham of the Admiralty Signal and Radar Establishment, England; Dr. A. M. Uttley of the Telecommunication Research Establishment, England; R. H. Harwood and Allen Huntington, working on tactical simulators at the Bureau of Ships Electronics Laboratory, San Diego; and J. J. Fleming, M. A. Richman, D. H. Gridley, and D. O. Larson of the Naval Research Laboratory.

Mr. C. W. Hargens visited the Laboratory to discuss material for his Bureau of Aeronautics report on missile simulation. Information was interchanged with Warren C. Doty of the University of Michigan on data conversion between analog and digital quantities.

Dr. R. M. Bowie of the Sylvania Laboratories inspected vacuum-tube facilities and discussed tube design problems.

APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were issued during May.

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
SR-5	Summary Report No. 5	16		2-48	
E-115	Testing and Modification of Bus Driver Circuit BA-1	4	3	5- 5-48	R. H. Gould
E-117	Filament Power Panel	1	1	5- 6-48	R. H. Murch
E-118	Rack Power Control Unit MOD 2	2	1	5- 6-48	R. H. Murch
E-119	Standard Pin Connections, Power Connector WWI	1	-	5-11-48	H. S. Lee
E-120	Power Wiring in WWI Repetitive Elements	4	-	5-12-48	C. W. Watt
E-123	Available Test Equipment	8	-	5-24-48	R.M.Fairbrother
M-349	Progress Report: An Investigation into the Reliability of the Capacitively-Coupled Flip-Flop	3	-	4-10-48	W. P. Horton
M-350	Progress Report: An Investigation into the Reliability of the Capacitively-Coupled Flip-Flop	3	-	3-15-48	W. P. Horton
M-357	Progress Report: Investigation of Electronic Computer Output Circuits	2	-	4-10-48	F. A. Foss
M-362	Grounding System for WWI	2	1	4-15-48	C. W. Watt
M-384	Discussion of Proposed Flip-Flop Register	3	1	4-28-48	H. Kenosian
M-385	Variable-Frequency Clock-Pulse Generator, Model 2	1	1	4-26-48	H. Kenosian
M-391	Painting of Panels for WWI	3	-	4-30-48	C. W. Watt
M-392	Signal Plate Assembly for ST-26 (Second 5" Storage Tube)	1	-	4-30-48	R. Shaw
M-393	Signal Plate Assembly for ST-27 (Third 5" Storage Tube)	1	-	4-30-48	R. Shaw
M-394	Conference with Eastman at MIT, April 21 & 22, 1948	5	-	5- 3-48	(H. R. Boyd (D. R. Brown
M-396	Preliminary Accumulator Test Specifications	5	-	5- 5-48	N. H. Taylor
M-397	Ohmeter Schedule for Checking WWI Accumulator Panels	4	-	5-12-48	H. L. Ziegle
M-398	Cathode-Follower Probe	1	1	5- 5-48	D. R. Brown
M-401	Check Register Checking	2	1	5- 5-48	R. P. Mayer
M-402	Panel-Selection Circuit Proposal, No. 2	2	2	5- 6-48	E. S. Rich
M-404	Relays for Voltage Variation Panels	1	-	5- 7-48	C. W. Watt
M-405	Progress Report: Coupling Circuits for a Storage-Tube Output System	2	-	5-10-48	C. Campling
M-410	Meeting of the Electronics Group, April 23 & May 7	1	-	5-12-48	S. Dodd

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
M-411	Control Pulse Delays	2	-	5-12-48	J. A. O'Brien
M-412	Multiplier Failure (Report 1)	1	-	5-13-48	N. Daggett
M-413	Check Register Checking	2	1	5-11-48	R. P. Mayer
M-414	Tube Socket Contact Material	1	1	5-13-48	C. W. Watt
M-415	Register Drivers and Video Cabling	1	-	5-14-48	H. Fahnestock
M-416	Bi-Weekly Report, Part I, May 14	18	-	5-14-48	
M-417	Bi-Weekly Report, Part II, May 14	17	-	5-14-48	
M-418	Evaporation Tube ET-35	2	-	5-14-48	R. Shaw
M-420	Switches	2	-	5-17-48	R. E. Hunt
M-421	R. F. Choke Specs.	1	-	5-17-48	C. W. Watt
M-423	Switching Time in Program Counter	2	-	5-18-48	R. R. Everett
M-424	Toggle Switch Storage; Switch Location	1	-	5-19-48	H. Fahnestock
M-426	Register Drivers	1	-	5-19-48	R. R. Everett
M-427	7AK7 Pin Contact	1	-	5-19-48	D. R. Brown
M-428	Fuse Indication Panel Prototype Construction Authorization	1	-	5-20-48	C. W. Watt
M-434	Storage Holding Stability Tests	5	13	5-21-48	J. W. Forrester
M-436	Test Equipment Calibration	1	-	5-24-48	H. R. Boyd
M-438	Power Feed to the Control Elements of WWI	1	-	5-24-48	C. W. Watt
M-439	Register Design Changes	2	-	5-25-48	H. Fahnestock
M-440	Coder	1	-	5-25-48	H. Kenosian
M-441	Program Register, Possible Omission of	2	-	5-25-48	R. R. Everett
M-447	Bi-Weekly Report, Part I, May 28	14	-	5-28-48	
M-448	Bi-Weekly Report, Part II, May 28	19	-	5-28-48	
C-50	Project Whirlwind Seminar No. 24: Runge-Kutta Method of Numerical Integration	3	-	5-3-48	P. Franklin
C-51	Runge-Kutta Method of Numerical Integration	3	-	5-5-48	P. Franklin