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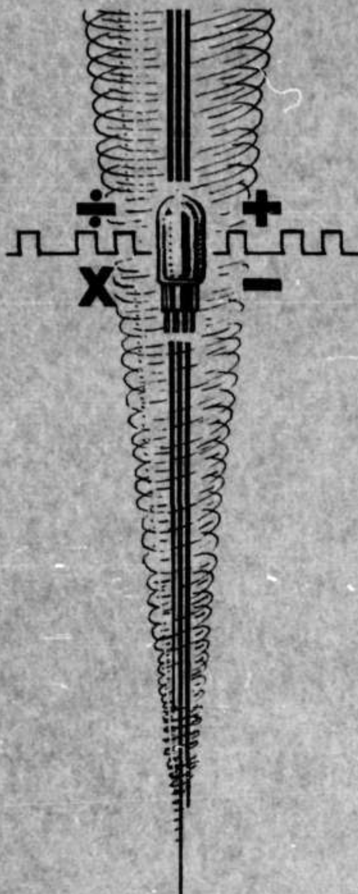

PROJECT WHIRLWIND

Contract N5ori60

SUMMARY REPORT No. 3

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

December, 1947

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SPECIAL DEVICES CENTER

CONFIDENTIAL

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 3

DECEMBER 1947

Submitted to the
SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
under Contract N5ori60

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

Project DIC 6345

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FOREWORD

PROJECT WHIRLWIND

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

THE WHIRLWIND COMPUTERS

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are: (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

REPORTS

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

TIME SCHEDULES

Time schedules for the WWI work are being revised, and corrected sets will be included in the February Summary Report. The time schedule on Page 15, Volume 1 of Summary Report 2, is based on information prepared in August and September, 1947. Since that time certain delays have occurred, making a revision necessary. Some electronic components of WWI have been delayed about two months while circuit research problems were being solved. In addition, the revised schedule will allow an additional two months safety factor in the estimates for electronic chassis construction. The new schedules call for completion of circuit construction about November, 1948, at about the same time as the storage and input and output units. Final testing will begin near the end of 1948 and will require approximately 6 months.

WHIRLWIND II

As indicated in Summary Report 2, Vol. 1, Page 7, the characteristics of WWII are indefinite at the present time. The time schedule therein, showing "WWII design" beginning in March 1948 and continuing beyond the end of the year, is in error; this section should have read: "Whirlwind II research". This indicates only a low level of activity in application studies and a continuation of basic circuit research. No contract or specifications have been written for Whirlwind II, and facilities are not at present available for design.

WHIRLWIND I

The repetitive elements (those used in each of the 16 digit columns) of Whirlwind I will be constructed by Sylvania Electric Products, Inc., of Boston, in the order in which they can most readily be incorporated into the system for test purposes. Thus, the arithmetic element, arithmetic control, and part of the test storage will be available before the complete control, and the last item will be the electrostatic storage and accompanying circuits. Aside from the electrostatic storage, the repetitive units included in the above consist of a total of about 200 panels of 10 different types, each containing from 8 to 20 vacuum tubes. Preliminary models of 7 of the 10 types have been constructed by Sylvania from preliminary circuit schematics furnished by M.I.T. As final circuit schematics are completed, Sylvania will make layouts and mechanical drawings for proposed prototypes. After approval of designs by M.I.T., the prototype will be constructed and tested and, after necessary modification, will serve as a model for production of the required quantities.

Final circuit schematics for the arithmetic element should be available in January, and for the control and test storage in February, though layouts for the latter need not be started as soon as the circuit schematics are completed. Those portions of the computer which are single units rather than repetitive will be constructed after the repetitive units are well under way.

Detailed circuit design for the electrostatic storage read-in, read-out, and deflection circuits has not yet been started; it will be undertaken by the electronic engineers who will become available as final circuit schematics of other parts of the system are turned over to Sylvania.

VISITORS

Visitors to the Project during December included Captain W. A. Corn of the Chief of Naval Operations Logistics Section, who is interested in the application of computers to supply and distribution problems. Representatives of North American Aviation, Inc., discussed with the Project possible applications of digital computers to guided-missile control.

SYSTEM DESIGN

A block-diagram outline of Whirlwind I has been in existence for several months, and electronic circuits have been designed which are capable of meeting the functional requirements of the block diagrams. However, the proposed computing speed of the machine is so high as to require additional detailed knowledge of the timing and synchronization of operations performed by individual circuits when they are integrated into large-scale systems.

TIMING STUDIES

To permit a study of system timing, operating times for each type of circuit to be used were determined by measurement, and the block diagrams were redrawn in terms of these specific circuits. Each pulse of a computing cycle was then traced through the entire computer plan. Since the time required for a pulse to reach a given piece of equipment could be predicted with reasonable accuracy, the synchronization of operations was readily checked. In several portions of the computer as originally visualized, pulses would have arrived at a circuit with too small a time interval between them, and in some places even in improper sequence. These difficulties were corrected by appropriate minor modifications in system design.

The time required for the basic flip-flop circuit to switch from one to the other of its stable states was found to be a limitation on the predicted maximum computing speed of the machine. Calculations showed that with present circuits the multiplication process could be safely performed no faster than the rate permitted by a time-pulse repetition frequency of two megacycles per second. This speed is considered adequate for Whirlwind I.

Although higher speeds are desirable, they can be attained only through very fundamental circuit improvements. Use of a radically different flip-flop circuit (see Circuits below) would offer some improvement, but this change will probably not be made in Whirlwind I because of the present advanced state of the design.

CIRCUITS

FLIP-FLOPS

"Flip-flop" circuits are fundamental computing units of electronic digital computers. Flip-flops presently used on the Whirlwind Project consist of two vacuum tubes with resistive coupling from the plate of each to the grid of the other. This type of intercoupling produces a device which has two stable states, since one or the other, but not both, of the tubes conduct at any one time. One of the two states may be used to represent the digit zero in the binary system of numbers, the other the digit one. A pulse to the common cathode connection always switches a flip-flop to the opposite state. A flip-flop may be set to a desired state by a pulse to the grid of either tube. The tube will be conducting if it has received a positive pulse, non-conducting if a negative pulse.

A simplified circuit-diagram of a common flip-flop (known as a d-c flip-flop) is shown in Fig. 1., page 4. When tube V_2 conducts, its plate current flows through resistor R_2, causing a voltage drop which lowers the potential of the plate terminal. Upon application of a pulse of appropriate polarity to one of the three input terminals, A, B, or C, regenerative switching action occurs and V_2 stops conducting. Its plate potential then rises exponentially to a higher value.

Direct connection between the plate of a flip-flop tube and a load circuit, for instance the grid of a gate-tube (Fig. 1), results in a high voltage level at the grid. This in turn requires that the gate-tube cathode be held at a high voltage level. For such cascading of circuits by direct coupling, many different well-regulated supply voltages are necessary.

Whirlwind circuits avoid this difficulty by using capacitive coupling between flip-flops and gate-tubes. A capacitor is inserted in the load-coupling lead at point D. Since the coupling capacitor passes only the incremental component of the plate voltage of a flip-flop tube, and not its absolute level, gate-tube cathodes can be grounded as is customary. However, capacitive coupling is usable only if the flip-flop is frequently switched from one position to the other, for otherwise the incremental charge on the coupling capacitor will leak off and the potential of the gate-tube grid will not always be indicative of flip-flop position. But a flip-flop must often represent a single binary digit for an indefinite period. To permit continual identification of the conducting tube at the load circuit, pairs of so-called restorer pulses are applied to the flip-flop, causing it to switch to the opposite position and then back again after one microsecond. Periodic application of these pulses maintains the necessary incremental charge on the coupling capacitor. Normal computing operations are suspended during their application, but computing speed is not materially affected. The time constant of the decay of the charge on the capacitor must, of course, be long relative to the time between pairs of restorer pulses. Germanium-crystal rectifiers are often connected between the load terminal of the condenser and a voltage source to maintain the desired absolute level of the load-circuit waveform.

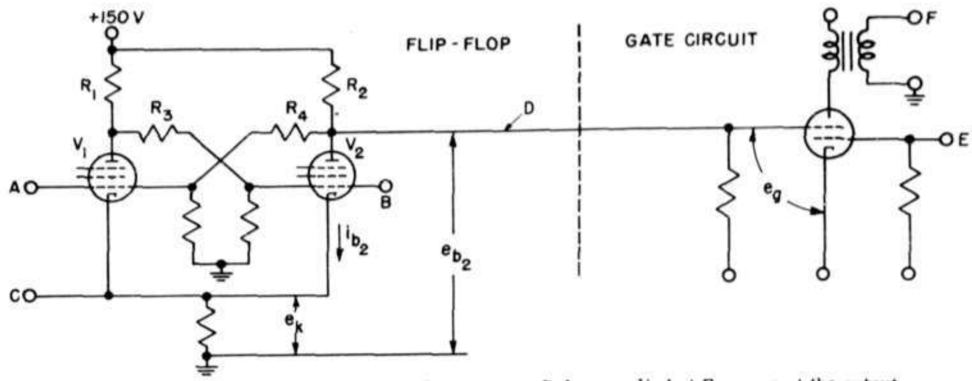

Fig. 1. Flip-flop and most common load circuit. Pulses applied at E appear at the output terminal, F, of the gate circuit, only when tube V_2 of the flip-flop is not conducting.

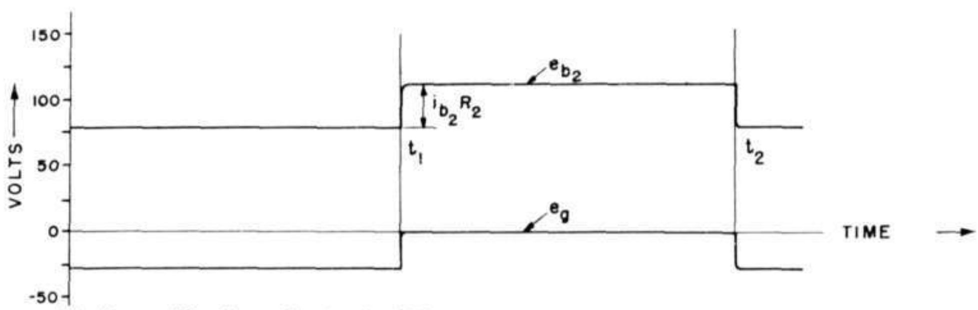

Fig. 2. Waveforms for circuit of Fig. 1. A positive pulse applied at A at time t_1 results in regenerative switching action which causes V_1 to conduct, V_2 to stop conducting. Between t_1 and t_2 the flip-flop represents a different binary number, and the gate circuit can pass a pulse applied at E. A positive pulse applied at B at time t_2 causes V_2 to conduct again, and the "gate" to close.

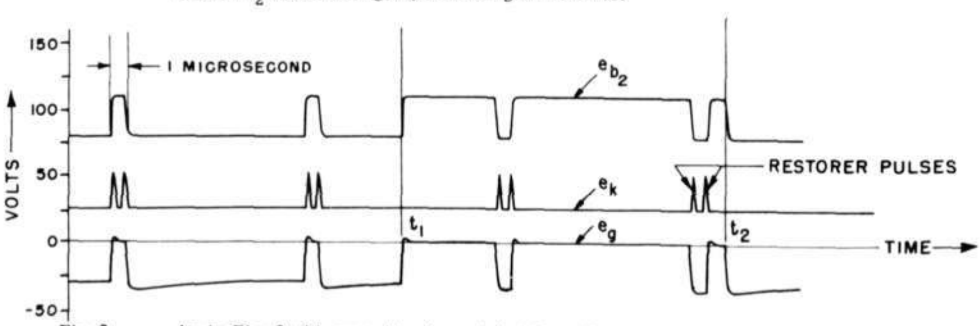

Fig. 3. As in Fig. 2 with capacitor inserted at D to block non-varying component of e_{b_2} from load circuit. The charge which leaks off the coupling capacitor is periodically restored by the action of restorer pulses applied at point C. (See waveform for e_k). Waveforms are essentially the same if R_3 and R_4 are replaced by capacitors, making an "a-c flip-flop".

Waveforms for direct and capacitive load coupling are shown in Figs. 2 and 3. To indicate the change in potential level at the gate-tube grid when the flip-flop is switched, a positive pulse is shown applied at point A at time t_1, and at point B at time t_2. The net gate-tube input voltage, e_g, is seen to be essentially the same for both direct and capacitive coupling except during the relatively short intervals required for restorer-pulse action. Except during those times, then, the voltage at the capacitively-coupled gate-tube grid is representative of the flip-flop position.

This scheme for capacitive coupling (commonly termed a-c coupling) of a flip-flop to a load circuit has suggested the possibility of capacitive intercoupling of the two tubes within the flip-flop. Such a circuit, which is similar to that of Fig. 1 but has capacitors in place of R_3 and R_4, does not inherently have the permanent digit-storage ability of the d-c flip-flop. It is actually a free-running multivibrator, and spontaneously tends to generate square waves. However, if pairs of restorer pulses are applied to it so that the time between pulse pairs is less than the natural period of the relaxation oscillations, the waveform at the gate-tube grid becomes essentially the same as for the d-c flip-flop (see Fig. 3). The restorer pulses maintain the charges on the internal coupling capacitors so that except during the restoring interval the circuit remains in one half-cycle of its natural oscillation. It may, of course, be switched to the other half-cycle by application of a pulse to one of the input terminals during the relatively long time between restoring intervals. Waveforms are essentially similar to those of Fig. 3.

This "a-c flip-flop" has been studied at some length with satisfactory results. The time required for a conducting tube to cease conducting in experimental models is appreciably less than the switching time of the d-c flip-flop (0.15 μsec, compared to 0.2 μsec), and the circuit does not have the undesirable sensitivity to inaccuracies in component values which is characteristic of the d-c flip-flop.

Although it appears very practicable, the a-c flip-flop has not yet been studied in sufficient detail to permit its use in Whirlwind I design. Whirlwind I can at some later date be converted to a-c flip-flops with little difficulty if desired.

STANDARDIZATION OF CIRCUITS

To prevent duplication of design efforts and to facilitate synthesis of computer systems, a set of diagrams for basic circuit types has been compiled. With whatever slight modifications as are dictated by particular applications, these basic gate-tube circuits, buffer amplifiers, flip-flops, gate generators, etc. are being used throughout Whirlwind I design wherever their individual functions are required.

In addition, future development of systems is to be facilitated by a line of standardized electronic test equipment for generating, gating, and distributing pulses at desired repetition frequencies. This equipment is being designed so that research engineers may, by rapid interconnection of various units, set up and experiment with sections of computer systems.

STORAGE TUBES

STORAGE SURFACE

The storage tubes that have been constructed for research studies fulfill many of the requirements of WWI. However the 30 microseconds consumed in storing a number is longer than desired and the large switching voltages must be reduced. Stability of the stored signals must be increased somewhat. These improvements depend primarily upon the development of a storage surface with adequate electrical properties. A surface employing a mosaic of conducting areas will probably be used to improve permanence of storage and prevent spreading of stored signals.

The emitting surfaces of alkali metals on silver used in television tubes and electron multiplier tubes have many of the desired characteristics. The technique employed in the production of these tubes might be used for storage tubes but requires distillation of the alkali in the final vacuum processing. This technique presents difficult problems of comtamination of the electrodes by the alkali metals. An easier assembly method is being sought in which the storage surface can be prepared before assembly into the storage tube.

Studies on secondary emitting conductors which can be deposited by evaporation have been conducted by Project Whirlwind staff members both at the Servomechanisms Laboratory and at the American Television Research Laboratories at Chicago. Drs. Lee De Forest and E. D. Carter of that Laboratory have made helpful suggestions.

TUBE CONSTRUCTION

During December, four tubes were constructed for studying storage phenomena, nine tubes for producing evaporated metal films, five tubes for studying secondary emission and life, and three for investigation of data storage in low-pressure gas discharge.

These tubes are all made of hard glass (nonex) and are sealed off without use of a getter. Processing is sufficiently thorough that no difficulty is encountered with gas emitted from tube surfaces.

Delays have been caused by a shortage of ten-pin nonex-presses used to support the electron guns and form the vacuum seals. Dies belonging to the supplier of these presses were destroyed by fire, and it has been necessary to design and construct new equipment.

COMPONENTS

7AK7 GATE TUBE

The circuits of WWI use such short-duration pulses (0.1 μsec) that time constants must be kept very small. Low impedance levels are therefore maintained, requiring high currents for satisfactory signal amplitudes. The only gate tube available until recently could not deliver sufficient current for many applications. However, a satisfactory design of a special high-current gate tube to replace the previously used 6AS6 was achieved by Sylvania Electric Products, Inc., late in November. The tube has been developed as a Company activity rather than as a Project Whirlwind activity. The design selected was test No. C-5245 of experimental type No. SR-1030. Selection was made after complete measurements had been obtained on a lot of 100 tubes. This particular design resulted in very few production losses. Production specifications were received and the tube was designated 7AK7 by the Radio Manufacturer's Association. The Project received 50 of the tubes and began using them for experimental work. Average characteristic curves and dissipation ratings are not yet available.

CRYSTAL RECTIFIERS

High-back-voltage germanium-crystal rectifiers are used throughout Whirlwind pulse circuits for pulse shaping and other purposes, and the Sylvania IN34 is adequate for most applications. An evaluation of crystal-rectifier reliability is being conducted at the present time with the cooperation of the Electronic Computers Section of the Bureau of Standards. All available data from the Whirlwind laboratory and the group at Sylvania are being collected.

Sylvania is now conducting life tests on seven different groups of special crystal rectifiers for use in a line-driving amplifier in Whirlwind I. This application requires very high peak forward current, approximately 500 milliamperes; inverse voltage is about 20 volts, and average forward current less than 15 milliamperes. The group at Sylvania feel that they can produce crystals which will be adequate. Life tests have been operating for between 800 and 2750 hours. A few crystals have exhibited a large decrease in back resistance, but this occurred early in life. Thirty of the most satisfactory crystal rectifiers, Sylvania No. D344, have been received for laboratory testing.

PULSE TRANSFORMERS

Many of the pulse circuits of Whirlwind I require transformers for such functions as impedance matching, polarity reversal, etc. Satisfactory pulse transformers have been designed. Two types have been found adequate for most applications: one with unity turns ratio, for inverting pulse polarity, and another with a 3:1 turns ratio, for both impedance matching and polarity inversion. They are used with 0.1-microsecond pulses of about 20-volt amplitude and repetition frequencies up to several megacycles.

Excluding mounting bases, these transformers occupy about 1/2 cubic inch of space. Single-layer primary and secondary windings take the form of two concentric cylinders of equal length. Proper turns ratio is achieved by use of wire sizes in that ratio. One leg of each C-shaped half of a ferromagnetic core is inserted into the coils, and the butt-jointed core halves are held together under pressure by a steel band. The cores are made, by Westinghouse Elec. & Mfg. Co., by winding a length of 0.001-inch hipersil (high-permeability silicon steel) ribbon about a rectangular mandrel, and are cut in two for convenience in adding the coils.

FIVE-DIGIT MULTIPLIER

The 5-digit multiplier is a prototype of 5 digits of the arithmetic element of WWI. Using a time-pulse repetition frequency of 2 megacycles per second, the unit multiplies two 5-digit binary numbers in 5 microseconds.

During preliminary test of this multiplier in November, it became apparent that specialized test methods were needed to study its operation. In particular it was necessary to observe in detail the wave shape of the output of any flip-flop, gate circuit, or buffer amplifier, and to study the time relationships which exist between the pulses which carry out the high-speed multiplication.

A "Multiplier Periodic Program Control" has been constructed to repeat multiplications each 1000 or 10,000 microseconds. Each multiplication is begun simultaneously with the start of the horizontal sweep of a cathode-ray oscilloscope, so that continuous viewing of circuit waveforms is possible.

After six weeks of multiplier operation, errors in computation have been noted which were traced to the gradual decrease in plate current of 6AG7 vacuum tubes in a 4-position crystal-matrix switch. This multi-position switch depends for its operation on balanced currents flowing in the four tubes which drive it. Unbalance of 20% to 30%, often obtained from random selection of commercial tubes, makes this circuit undependable. A "whiffletree" gate circuit has been substituted for this matrix switch. Its operation has been successful and to date without computational error. Since no balanced currents are required, demands on vacuum tubes are much less stringent.

MATHEMATICS

The Office of Naval Research and the Special Devices Center have requested that mathematical work on Project Whirlwind be broadened. Professor Franklin, head of the Project mathematics work, has contacted about 25 mathematics groups throughout the country in search of suitable talent. A few prospects have been located. The mathematics staff will be expanded as suitable men are located, and as soon as the Project Whirlwind contract is adjusted to cover continuing basic research programs.

The principal subjects being considered by the mathematics group are coding, the solution of linear algebraic equations, and methods of numerical integration.

A comparison of the Blaess procedure with that of Runge-Kutta has shown the latter decidedly superior for the step-by-step integration of ordinary differential equations.

Of the standard methods for the solution of linear algebraic equations, the Crout method is so far the most promising, as it seems to require the least storage and shortest time. A comparison of the Doolittle method with the Crout method indicates that for the solution of symmetrical systems the two are algebraically identical. The geometrical arrangement used by Crout may, however, be more suggestive for the formulation of a code.

Recent investigations have been made of the optimum distribution of intervals in a table for minimum error in linear interpolation. It was found that the maximum possible error is inversely proportional to the square of the number of intervals in a given range. If desirable, a study of higher degree interpolation along the same lines will be made at a later time.

Effort has been directed toward understanding planning and coding procedures so that consideration may be given to the question of maintaining a suitable scale factor throughout the solution of a given problem.

The importance of preventing loss of significant figures through overflow or round-off can hardly be overestimated, and some procedures should probably be established for typical problems.

The machine can, through proper programming, be required to adjust scale factor either continuously or at preselected critical times. Critical readjustment is indicated, but just how mathematical methods and physical intuition can best be used in the preselection process is not immediately apparent and will be investigated further, as will methods of ordering the readjustment.

Timing studies recently completed (see SYSTEM DESIGN) should be of considerable use in analyzing time factors in various possible coding procedures.

TROUBLE LOCATION

Because digital electronic computers contain many thousands of electronic-circuit components, failures must be expected. Such failures almost always cause errors in computation, and temporarily destroy the usefulness of the machine. Rapid trouble-location methods are therefore of great importance.

A scheme which has been proposed for facilitating the location of faults in WWI uses prepared groups of test problems whose answers are known. These problems are of two types:

1) Check problems, solved periodically, designed to use as much of the machine as possible. Errors in solutions will indicate that some part of the machine is not functioning correctly.
2) Trouble-location problems, designed to use only small portions of the machine. Errors in the solution of one or more of a series of these problems will provide information on the location of a fault after its existence has been demonstrated by an error in the solution of a check problem.

The machine itself may thus be made to locate faults which would require exorbitant time by manual methods. Simultaneous failure of many elements, or failure of certain critical elements, will result in greater difficulty, but such occurrences should be few relative to the total number of failures.

Although primarily intended as a means for finding steady-state faults due to the complete failure of a component, this scheme will be extended to finding of marginal components whose complete failure is imminent, which might be causing random errors. It is expected that such components can be made to give steady-state indications of failure by appropriate variation of circuit supply voltages and of the repetition frequency of applied pulses.

As an example, for certain types of faults, if the voltage of the screen-grid in a marginally operating vacuum tube is lowered slightly, complete failure can be produced, permitting discovery by check problems and subsequent location by trouble-location problems.

Whirlwind I power-supply systems are therefore being designed to permit selective variation of supply voltages in a range above and below normal operating values. The added complexity of cabling and the additional equipment required for this purpose are believed well justified by the expected gain in computing reliability.

INPUT AND OUTPUT

CONVERSION DEVICES

The purposes of conversion devices in control and simulation systems are:

1) To convert electrical and mechanical data (for example, position of the pilot's controls in the cockpit of an aircraft analyzer) to binary coded numbers.
2) To convert computed binary numbers (for example, altitute or air-speed) into physical quantities to be observed, or to operate physical equipment.

The conversion must be rapid and, in some cases, very precise.

Study at present is concentrated on conversion methods requiring high precision, say 1 part in 4000, since these present the most difficult problems. To date, methods of converting shaft rotation or analog voltages to binary numbers have been outlined. No sufficiently precise method of converting a binary quantity to an analog quantity directly has yet been found. It seems probable that the binary-to-analog conversion will have to be performed by a closed-cycle system using an analog-to-binary converter in the feedback loop.

FILM READER RECORDER

Interconnection between the computer and the film reader-recorder being developed by Eastman Kodak has been discussed by Eastman and Project Whirlwind personnel. Whirlwind I will have two registers used both for supplying data to and receiving data from the film units. One of them will hold a number, the other its complement. Since the two registers may be compared, the operations of reading and writing are completely and continuously checked.

MAGNETIC TAPE RECORDING

One staff member is studying magnetic tape recording. Although WWI will first be constructed with photographic input and output, erasable magnetic storage may later be required for some applications.

Apparatus for recording pulse signals on a magnetic tape has been constructed; it is being modified in accordance with the indications of preliminary tests.

The design of a head that will obtain readings from a stationary tape shows some promise. The principle used is to produce a change of inductance in the head by a magnetized spot on the tape, and then to detect the change of inductance with a bridge circuit.

SIMULATION

CONTROL-FORCE SIMULATION

The present control-force simulation program is aimed toward design and construction of a full-scale test model of the control-force hydraulic servomechanism. This model is to be tested and studied and should be suitable as an element for the first testing of a complete aircraft simulator system.

One of the most difficult problems in the servo development is the design of a sufficiently accurate and sensitive device which will produce a differential pressure proportional to its input signal. A new differential-pressure regulator has been designed and is now under construction. Static tests are scheduled for next month.

COCKPIT

The present cockpit program calls for design and construction of a simplified laboratory cockpit for use in evaluation of the computer application to aircraft stability and control analysis. Simulation of flight conditions and aircraft environment should be as accurate as possible. However, motion of the cockpit (except for simulated vibration) will not be attempted at present.

Study of control-system elements to simulate backlash, coulomb friction, and elastance is progressing, but probably will not be incorporated into the first model.

SAMPLING SERVO

The general theory of servomechanisms operating from intermittent input signals is being studied as time permits. Since the available knowledge and experience in this field is considerably less than in the field of continuous servos, a better understanding of general theory should precede any attempts at specific designs.

APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were issued during December.

No.	Title	Date	Author
	Summary Report No. 2	11-47	
R-126	Step Counter for 5-Digit Multiplier (Abstract in E-67)	8-29-47	E.I.Blumenthal
R-128	The Embossing and Anodization of Aluminum for Storage Tube Dielectric Surfaces (Abstract in E-72)	7-8-47	J.R. Macdonald
R-129	Conversion of Shaft Position to Binary Code (Abstract in E-85)	10-15-47	H. P. Stabler
R-130	Potential Plotting with an Electrolytic Tank (Abstract in E-65)	7-22-47	J.R. Macdonald
R-131	The Physical Characteristics of Aluminum Oxide Dielectric Layers. (Abstract in E-74)	7-23-47	J.R. Macdonald
R-132	Storage Tube Secondary Electron Control with a Magnetic Field (Abstract in E-70)	10-16-47	J.R. Macdonald
E-77	Blackout in 6AS6 and SR-1030 Gate Tubes	12-1-47	R. L. Best
E-78	Standard Test Equipment Program	12-4-47	J. O. Ely
E-79	Proposed Specifications WWI	12-10-47	H. Fahnestock
E-80	Circuit Standardization	12-11-47	J. A. O' Brien
E-82	2:1 - 4:1 Binary Frequency Divider	12-12-47	H. Kenosian
E-83	Multiplier Life Data	12-12-47	J. J. O' Brien
E-84	Model II Crystal Tester	12-16-47	D. J. Crawford
E-86	Single Pulse Synchronizer	12-16-47	H. Kenosian
M-137	Computer Codes for WWI	11-4-47	R.R. Everett
M-167	Electrolytically Produced Oxide Protective Layers on Aluminum (H. Rohrig)	11-20-47	M.I.Florencourt
M-171	The Siemens-Scheckert Vacuum Evaporation Methods Applied to Large First Surface Mirrors (In part) copied from microfilm	11-28-47	M.I.Florencourt
M-173	Standard Test Equipment	12-4-47	J.W.Forrester
M-175	Hydraulic Servomechanism for Cockpit Tilting	12-5-47	C. R. Wieser
M-179	Meeting at Eastman-Kodak's Hawk-Eye Plant December 4, 1947	12-11-47	D. R. Brown
M-185	Bi-Weekly Report Part I. December 15, 1947	12-15-47	
M-186	Bi-Weekly Report Part II. December 15, 1947	12-15-47	
M-192	Flip-Flop Life Test Rack Run No. 3	12-18-47	J. J. O'Brien
M-202	Bi-Weekly Report Part I. December 26, 1947	12-30-47	
M-203	Bi-Weekly Report Part II. December 26, 1947	12-30-47	