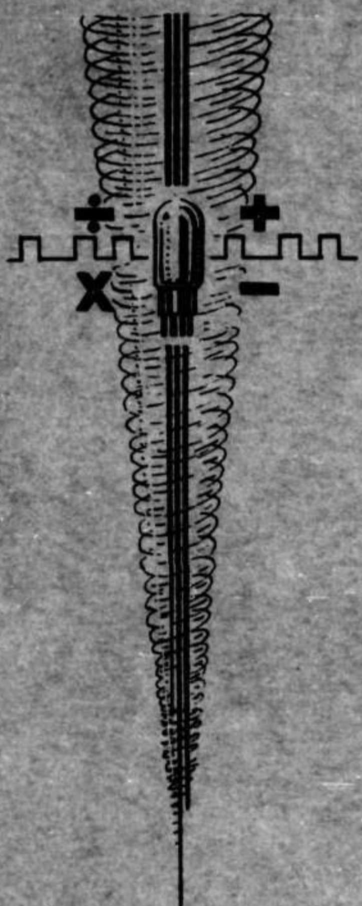


PROJECT WHIRLWIND

Contract N5ori60

SUMMARY REPORT NO. 5

FEBRUARY, 1948

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Copy 33

~~CONFIDENTIAL~~ Unclassified per letter 1/23/50

SPECIAL DEVICES CENTER

CONFIDENTIAL

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 5

FEBRUARY 1948

Submitted to the
SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
under Contract N5ori60

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

Project DIC 6345

TABLE OF CONTENTS

FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

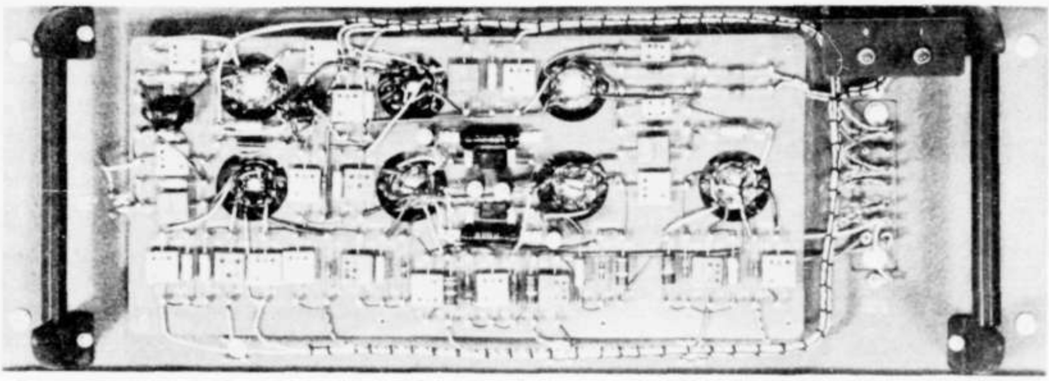
Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

WHIRLWIND I LAYOUT AND CONSTRUCTION

Final circuit schematics of the A-register zero digit and of the B-register have been released to Sylvania for layout of the Whirlwind I prototypes. This completes the arithmetic element releases, since the accumulator prototype is to be laid out and constructed at MIT.

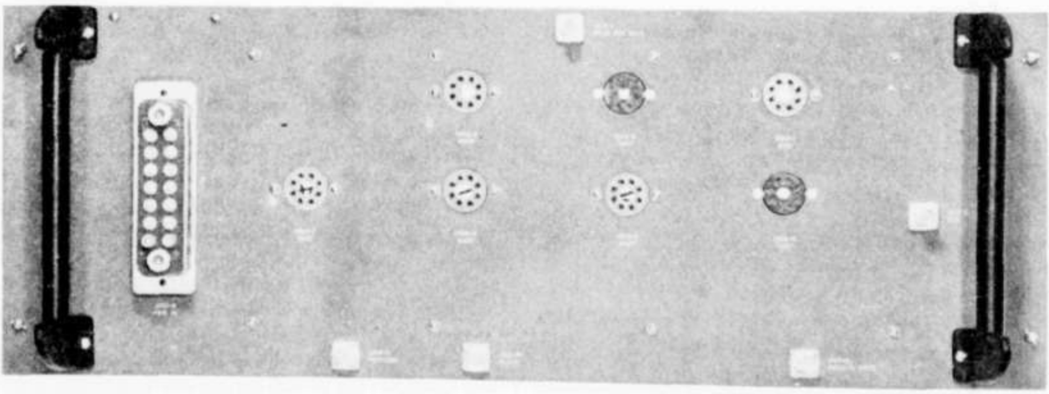
Sylvania has furnished preliminary video layouts for the A-register and B-register. These have been slightly modified by MIT and returned for completion of production drawings from which prototypes will be constructed.

Sylvania has delivered the sample program register prototype shown in the accompanying photographs. This has served a very useful purpose in freezing designs, and with minor modifications agreed on by MIT and Sylvania will become the standard for design of the Whirlwind I repetitive units.



PROTOTYPE PANEL, PROGRAM REGISTER DIGIT - FRONT VIEW

The construction of this panel is typical of all the register panels in the computer. All components and connections are accessible for test while the machine is running. Each digit panel is individually removable for service or modification.



PROTOTYPE PANEL, PROGRAM REGISTER DIGIT - BACK VIEW

As in the other repetitive units of Whirlwind I, all tubes, video cables, and power connectors are mounted on one side of the panel to facilitate replacement in case of failure.

PROJECT STAFF

New Staff Members

The following joined the Project Whirlwind staff in February:

Louis J. Nardone, working on storage tube deflection circuits. Mr. Nardone is a graduate of Northeastern University, January 1948, B.S. Electrical Engineering. He served with the Army Signal Corps, 1943-1946.

John S. Rochefort, working with the storage tube group. Mr. Rochefort is a graduate of Northeastern University, January 1948, B. S. Electrical Engineering. He served with the Army Signal Corps, 1943-1946.

John M. Hunt, with the electronics group. Mr. Hunt is a graduate of the University of Kansas, January 1948, B. S. Engineering and Physics. He worked as a radio engineer with TWA, 1940-1943, and served with the Naval Air Force as electronics officer, 1943-1945.

Monson H. Hayes, Jr., with the electronics group. Mr. Hayes is a graduate of the University of Maine, January 1948, B.S. Electrical Engineering. Served with the Navy, 1944-1946.

Rollin P. Mayer, on block diagrams. Mr. Mayer is a graduate of Northeastern University, January 1948, B.S. Electrical Engineering. Served with the Navy, 1945-1946.

William P. Horton is doing research for a thesis on the a-c flip-flop, carrying on work that was being done by his brother.

Frederick Foss is doing thesis research on output printers.

VISITORS

During February Dr. John von Neumann of the Institute for Advanced Study visited the Laboratory on three days to discuss the nature of the Whirlwind computer and its applications. The classes of control and simulation problems examined were those in which computing sequences are short and in which round-off and truncation errors are unlikely to be important. Technical status of the computer was reviewed and machine arrangement, block diagrams, and utilization discussed.

Dr. Mina Rees, Mathematics Branch of ONR, and Dr. John Curtiss and Dr. H. D. Huskey of the Bureau of Standards, considered in some detail with Project Whirlwind staff the nature of engineering problems of computer design and the successive stages of development leading to a final product.

R. L. Snyder, in charge of computer activity on the EDVAC at the University of Pennsylvania, exchanged information on computer status and engineering details. Mr. R. Benjamin of the British Admiralty and J. H. Kerfoot and Lt. Belyea of the Canadian Navy discussed insofar as clearances permitted the applications of digital computers to simulation and military control. Both organizations have activity and work in these fields.

Captain Johns, Commander Thompson, and Dr. C. F. Muckenhaupt of the Boston office of ONR visited the Servomechanisms Laboratory.

VISITS

Project members inspected vacuum tube construction methods and discussed processing of the 7AK7 gate tube with Sylvania Electric Products at Emporium, Pennsylvania. In connection with the storage tube work, cooperation and helpful advice were obtained thru a visit to the Corning Glass Works at Corning, New York.

Mr. F. S. Rich attended the conference on recording and reduction of data from the tracking of aircraft targets and guided missiles which was sponsored by the Army Ground Forces at Fort Bliss, Texas.

TIME SCHEDULES

Individual time schedules have been drawn up for principal components of the Whirlwind I computer and work in connection with the construction of the computer.

The time schedules have been divided into three major classifications:

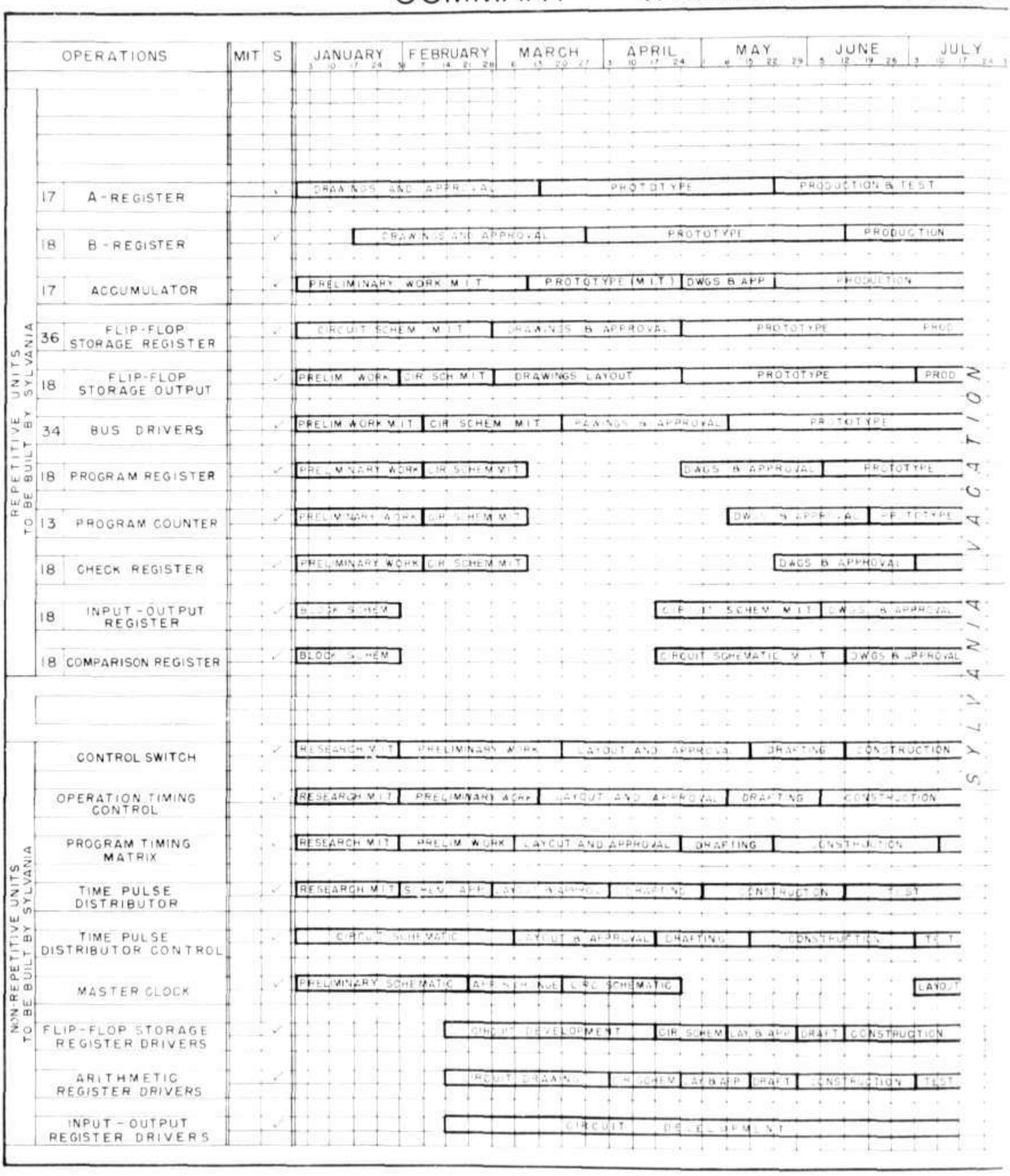
1. Repetitive Units.
2. Non-Repetitive Units.
3. Others.

In general the first two classifications include the schedules of all the components being constructed by Sylvania Electric Products, Inc., under subcontract. The third classification includes all other schedules.

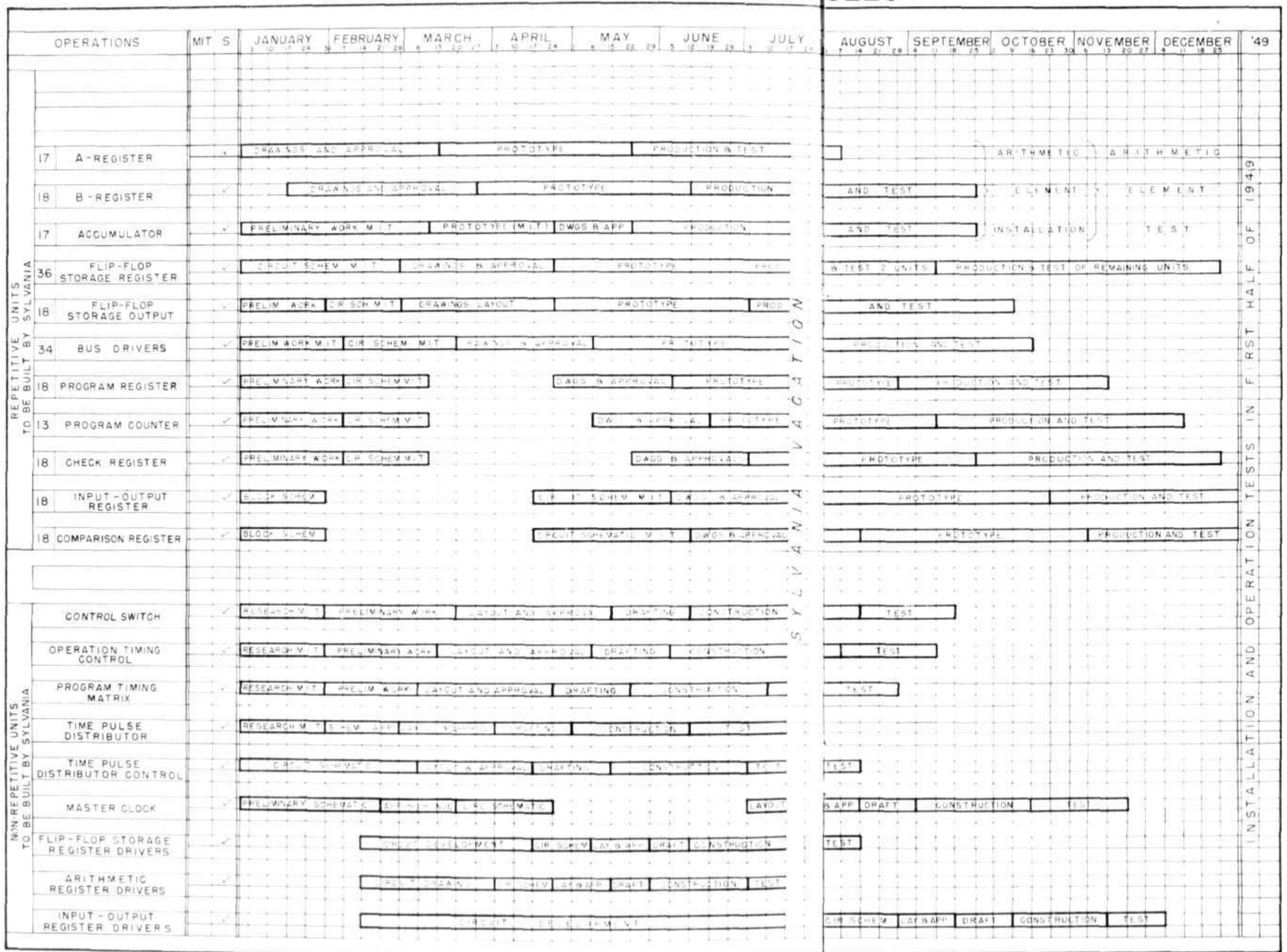
In addition, the individual schedules have been consolidated into one Summary Schedule shown on pages 4 and 5 of this report.

All schedules will be posted bi-weekly or monthly to show status and progress. Beginning in the next Monthly Summary Report, the summary schedule (pages 4 and 5) will be posted to show the status of work at the end of the month.

SUMMARY - WHIRLWIND I SCHED

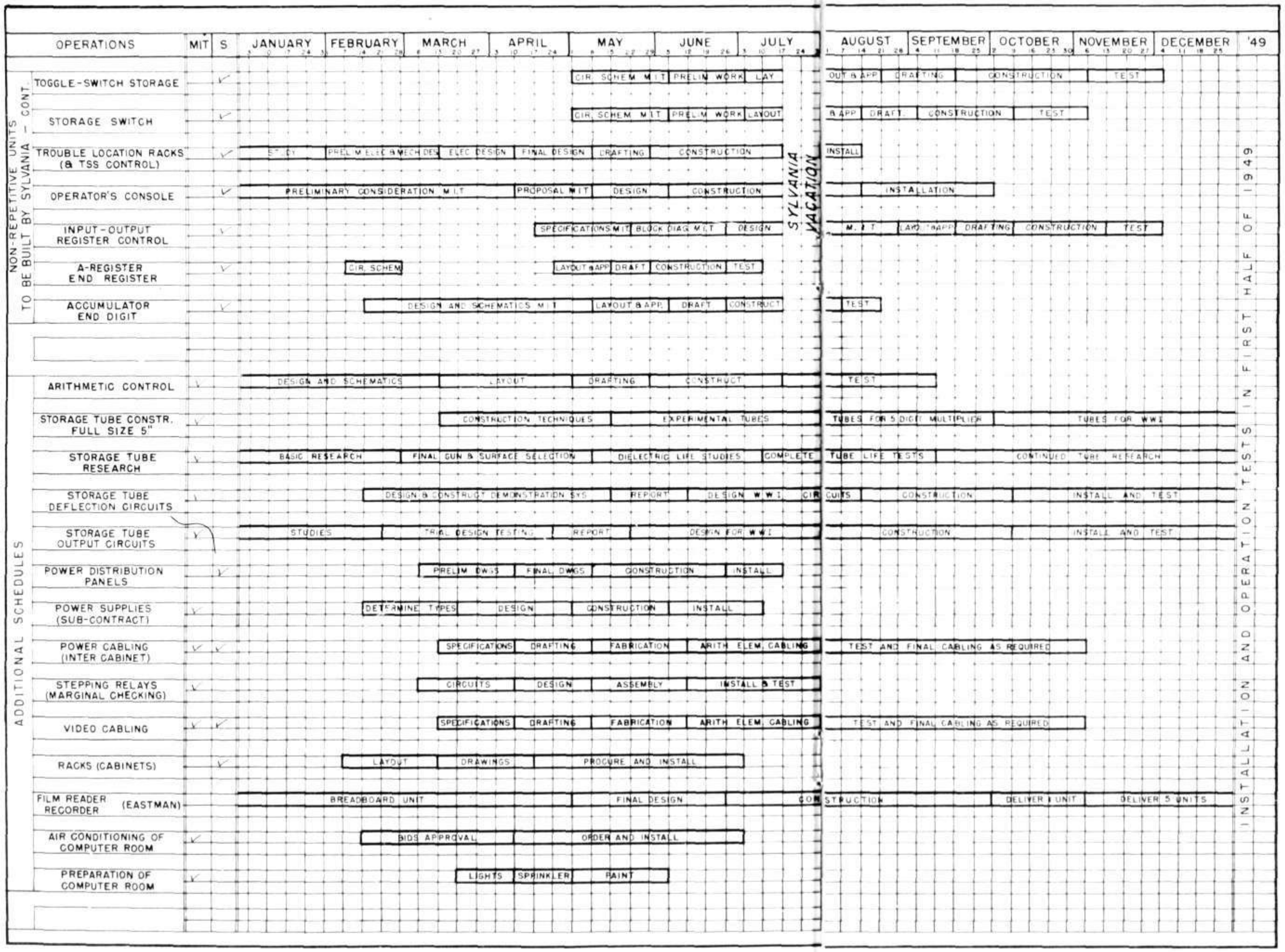


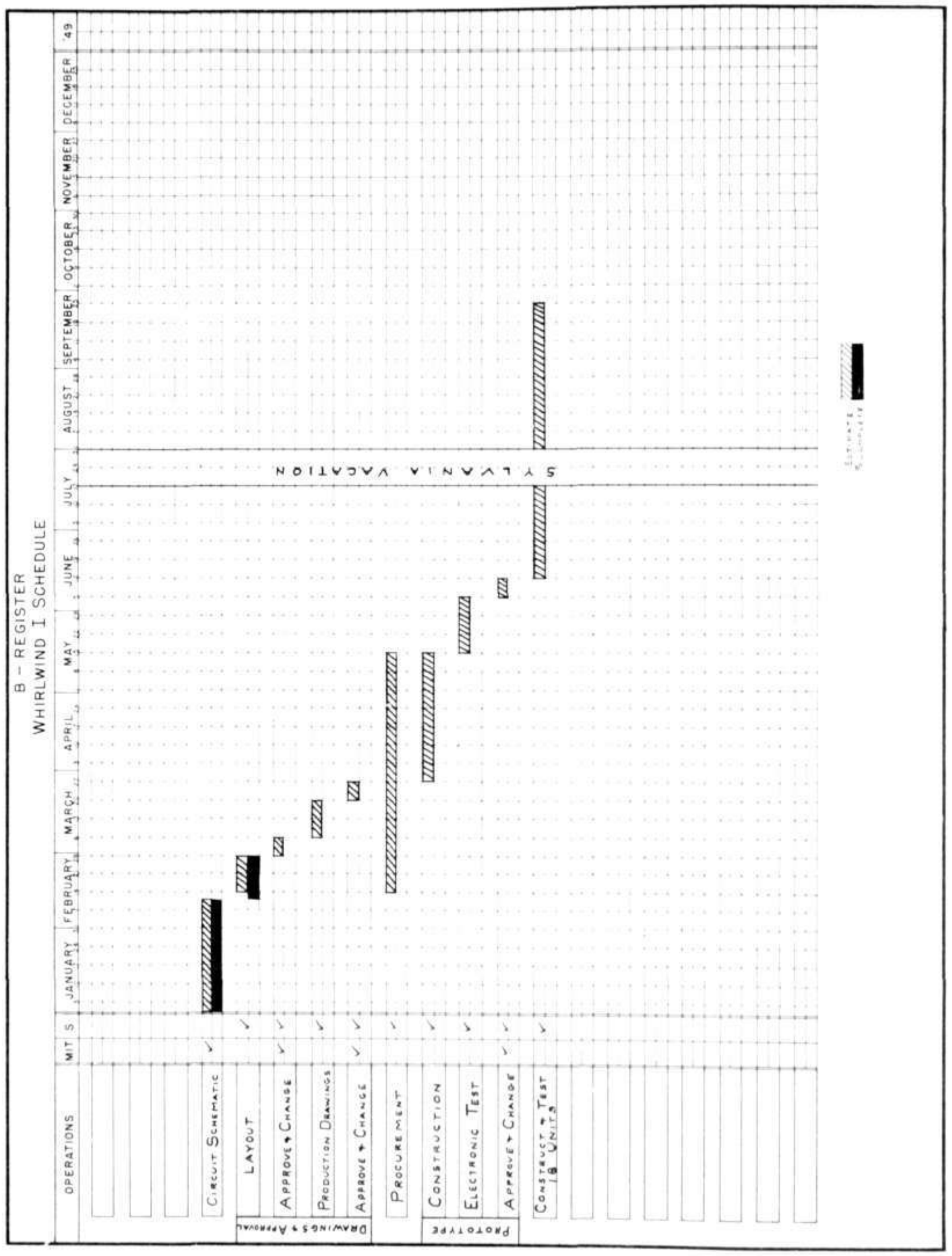
SUMMARY - WHIRLWIND I SCHEDULES

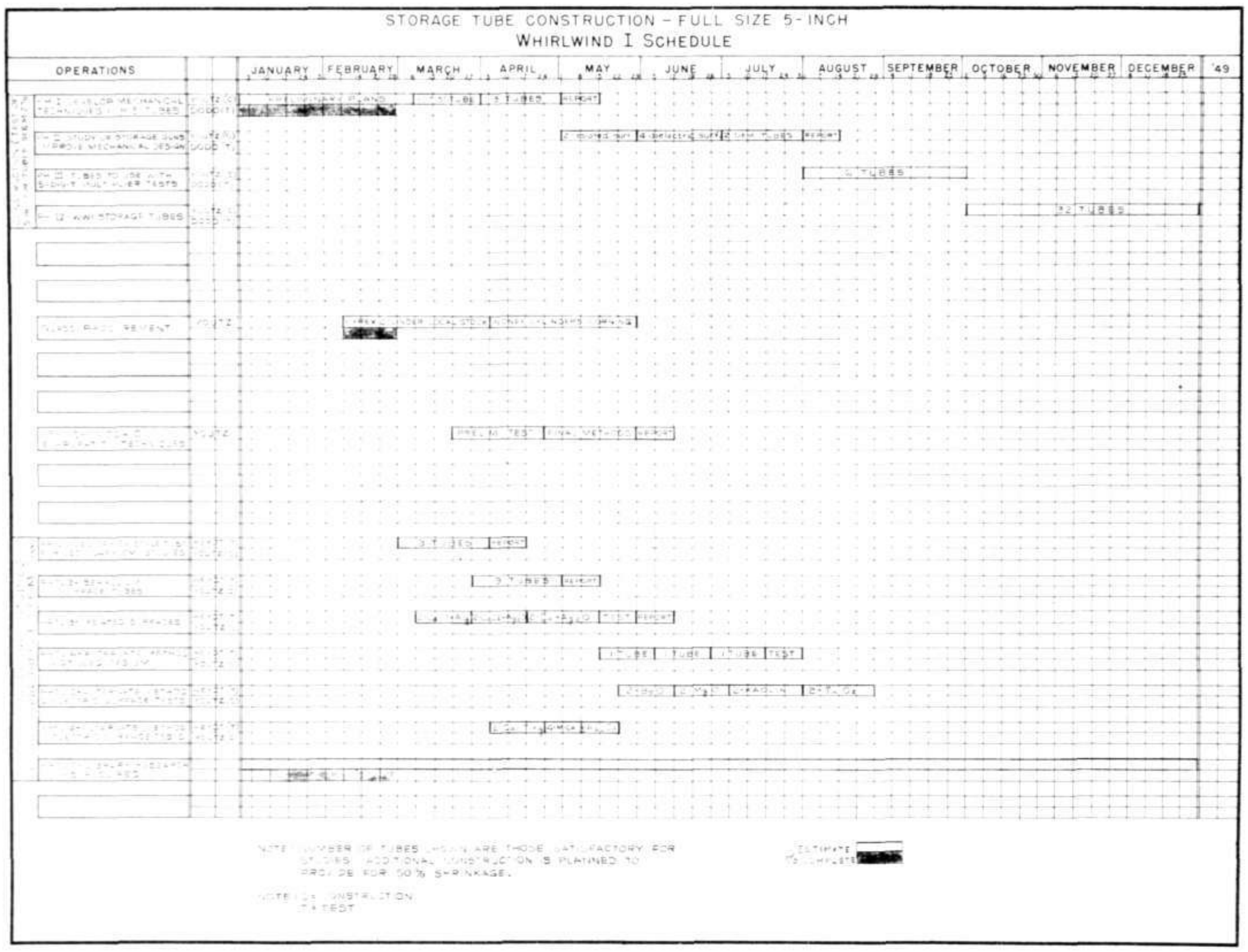


APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

SUMMARY – WHIRLWIND I SCHEDULES CONT.




B - REGISTER
WHIRLWIND I SCHEDULE
OPERATIONS
MIT
S
JANUARY
FEBRUARY
MARCH
APRIL
MAY
JUNE
JULY
AUGUST
SEPTEMBER
OCTOBER
NOVEMBER
DECEMBER
'49
Circuit Schematic
Layout
Approve + Change
Production Drawings
Approve + Change
Procurement
Construction
Electronic Test
Approve + Change
Construct + Test 18 Units
Drawings + Approval
Prototype
SYLVANIA VACATION


STORAGE TUBE CONSTRUCTION - FULL SIZE 5-INCH
WHIRLWIND I SCHEDULE
OPERATIONS
JANUARY
FEBRUARY
MARCH
APRIL
MAY
JUNE
JULY
AUGUST
SEPTEMBER
OCTOBER
NOVEMBER
DECEMBER
'49

PROJECT STAFF

New Staff Members

The following joined the Project Whirlwind staff in February:

Louis J. Nardone, working on storage tube deflection circuits. Mr. Nardone is a graduate of Northeastern University, January 1948, B.S. Electrical Engineering. He served with the Army Signal Corps, 1943-1946.

John S. Rochefort, working with the storage tube group. Mr. Rochefort is a graduate of Northeastern University, January 1948, B. S. Electrical Engineering. He served with the Army Signal Corps, 1943-1946.

John M. Hunt, with the electronics group. Mr. Hunt is a graduate of the University of Kansas, January 1948, B. S. Engineering and Physics. He worked as a radio engineer with TWA, 1940-1943, and served with the Naval Air Force as electronics officer, 1943-1945.

Monson H. Hayes, Jr., with the electronics group. Mr. Hayes is a graduate of the University of Maine, January 1948, B.S. Electrical Engineering. Served with the Navy, 1944-1946.

Rollin P. Mayer, on block diagrams. Mr. Mayer is a graduate of Northeastern University, January 1948, B.S. Electrical Engineering. Served with the Navy, 1945-1946.

William P. Horton is doing research for a thesis on the a-c flip-flop, carrying on work that was being done by his brother.

Frederick Foss is doing thesis research on output printers.

VISITORS

During February Dr. John von Neumann of the Institute for Advanced Study visited the Laboratory on three days to discuss the nature of the Whirlwind computer and its applications. The classes of control and simulation problems examined were those in which computing sequences are short and in which round-off and truncation errors are unlikely to be important. Technical status of the computer was reviewed and machine arrangement, block diagrams, and utilization discussed.

Dr. Mina Rees, Mathematics Branch of ONR, and Dr. John Curtiss and Dr. H. D. Huskey of the Bureau of Standards, considered in some detail with Project Whirlwind staff the nature of engineering problems of computer design and the successive stages of development leading to a final product.

R. L. Snyder, in charge of computer activity on the EDVAC at the University of Pennsylvania, exchanged information on computer status and engineering details. Mr. R. Benjamin of the British Admiralty and J. H. Kerfoot and Lt. Belyea of the Canadian Navy discussed insofar as clearances permitted the applications of digital computers to simulation and military control. Both organizations have activity and work in these fields.

Captain Johns, Commander Thompson, and Dr. C. F. Muckenhaupt of the Boston office of ONR visited the Servomechanisms Laboratory.

VISITS

Project members inspected vacuum tube construction methods and discussed processing of the 7AK7 gate tube with Sylvania Electric Products at Emporium, Pennsylvania. In connection with the storage tube work, cooperation and helpful advice were obtained thru a visit to the Corning Glass Works at Corning, New York.

Mr. E. S. Rich attended the conference on recording and reduction of data from the tracking of aircraft targets and guided missiles which was sponsored by the Army Ground Forces at Fort Bliss, Texas.

TIME SCHEDULES

Individual time schedules have been drawn up for principal components of the Whirlwind I computer and work in connection with the construction of the computer.

The time schedules have been divided into three major classifications:

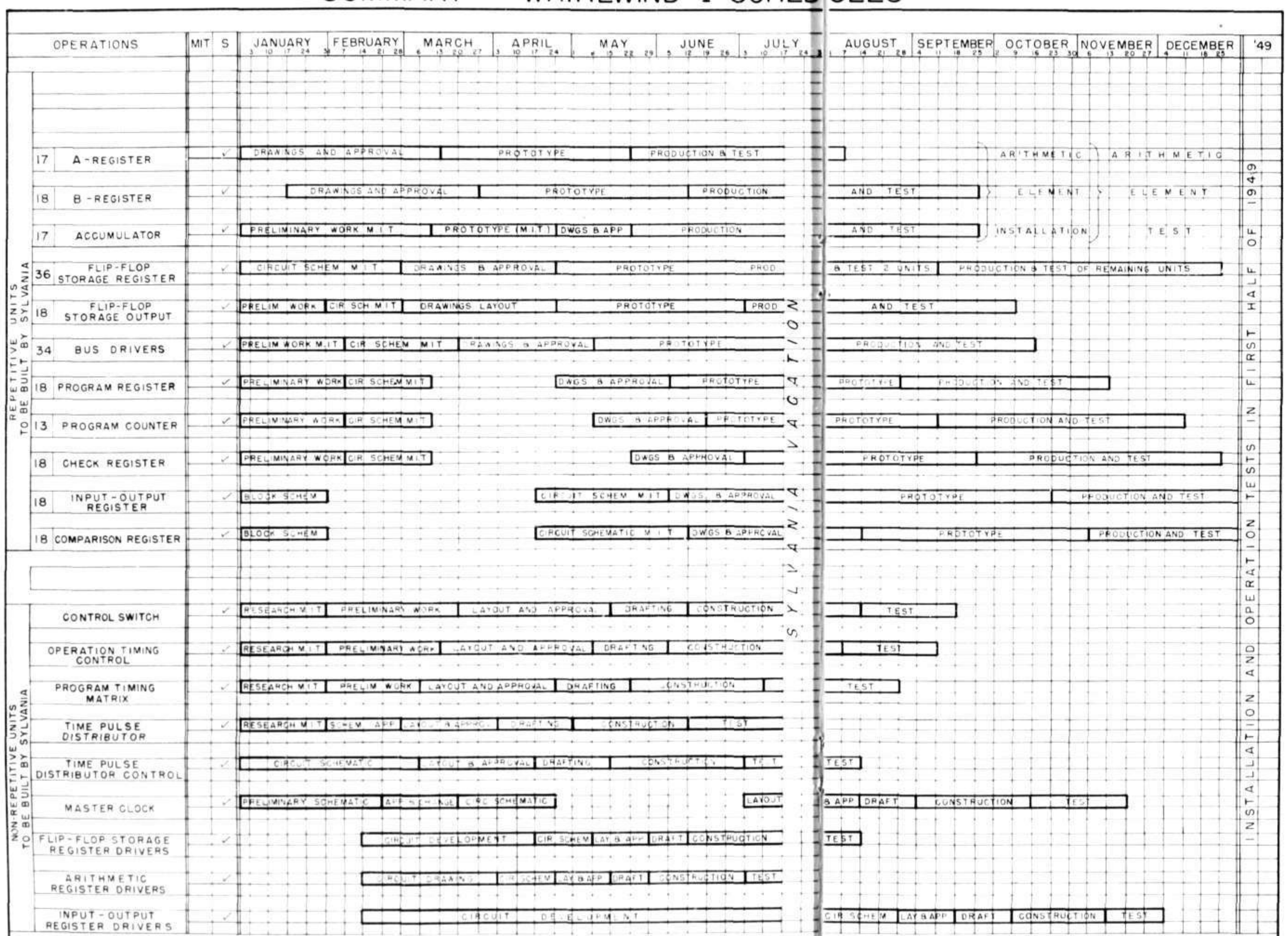
1. Repetitive Units.
2. Non-Repetitive Units.
3. Others.

In general the first two classifications include the schedules of all the components being constructed by Sylvania Electric Products, Inc., under subcontract. The third classification includes all other schedules.

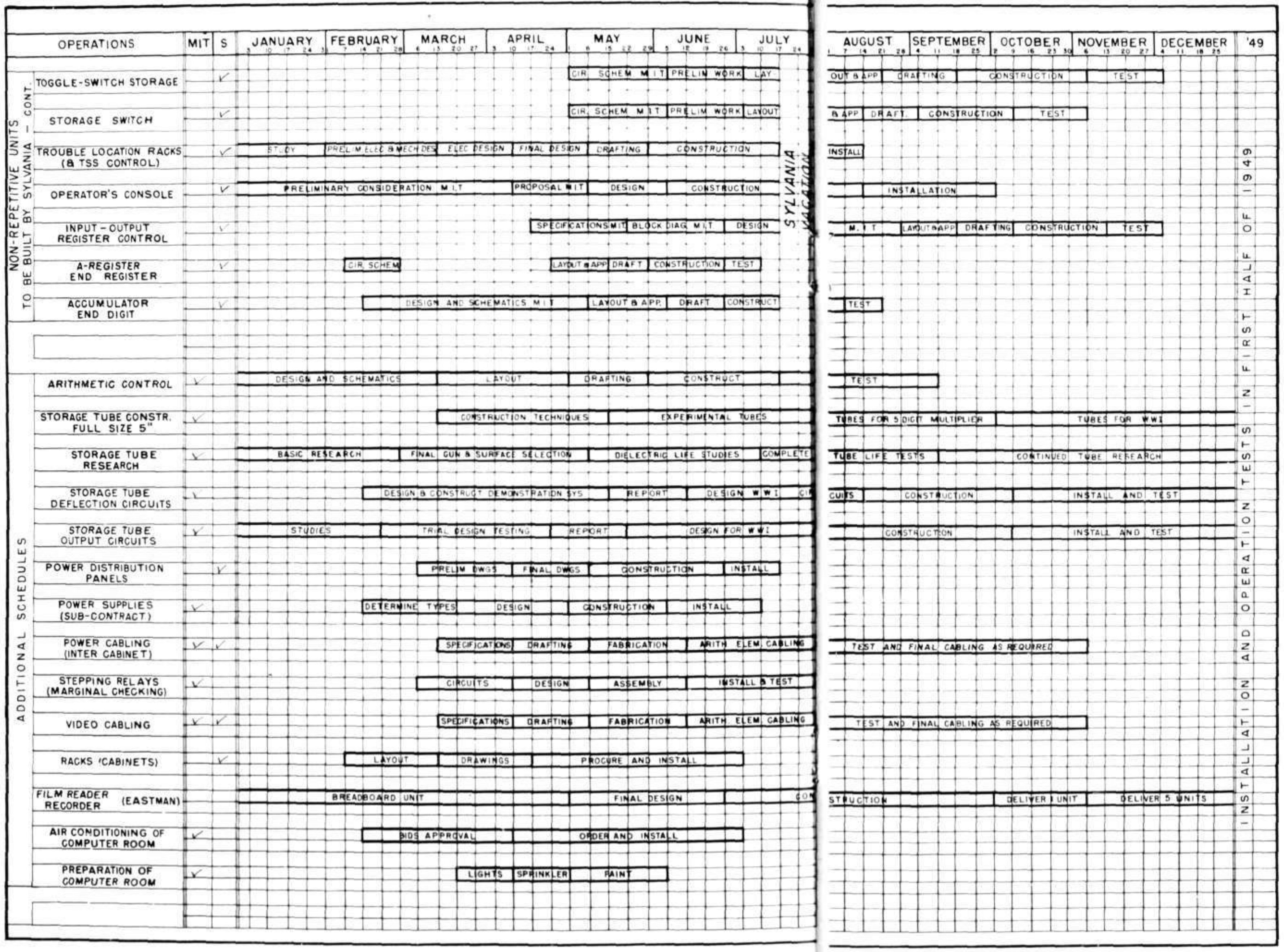
In addition, the individual schedules have been consolidated into one Summary Schedule shown on pages 4 and 5 of this report.

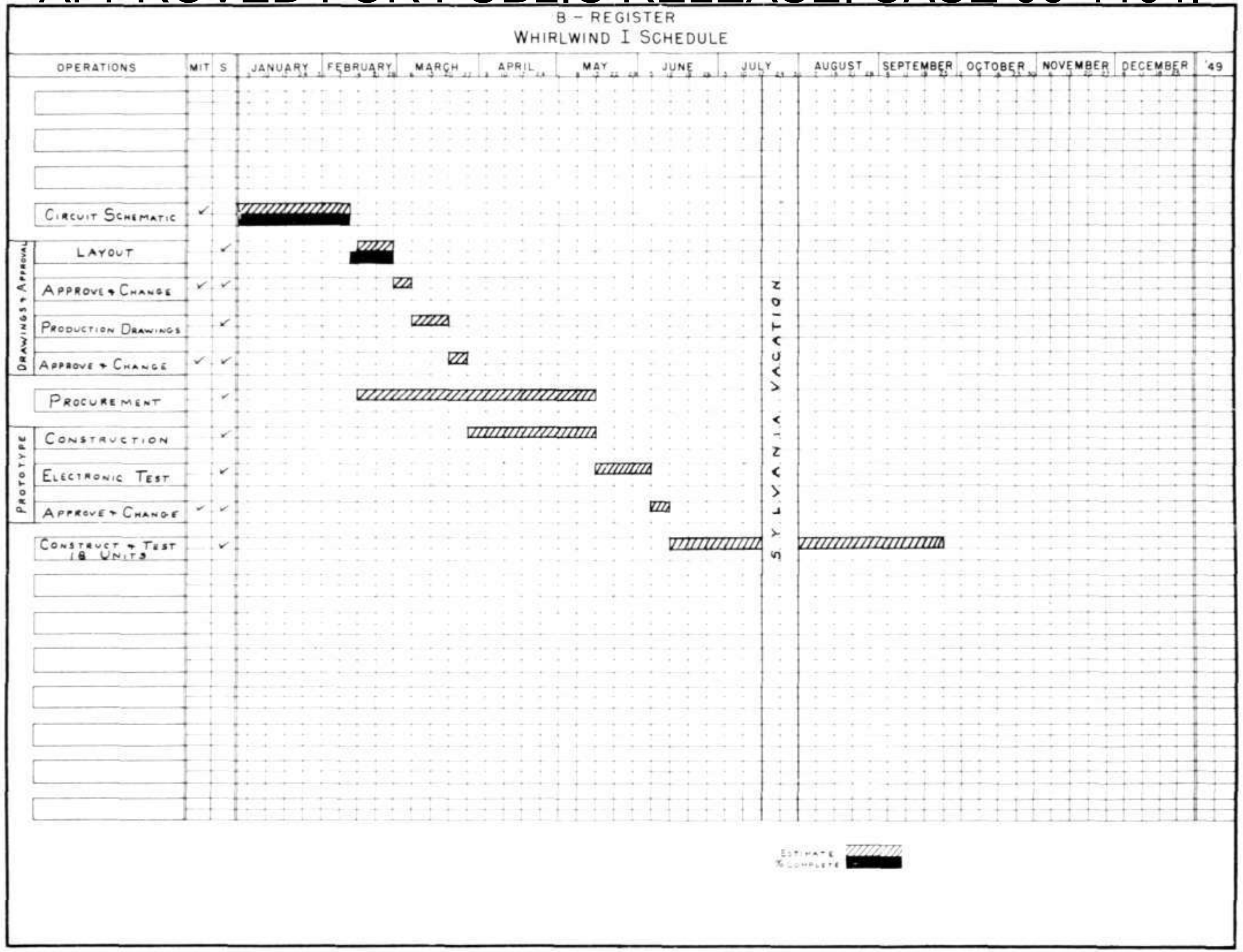
All schedules will be posted bi-weekly or monthly to show status and progress. Beginning in the next Monthly Summary Report, the summary schedule (pages 4 and 5) will be posted to show the status of work at the end of the month.

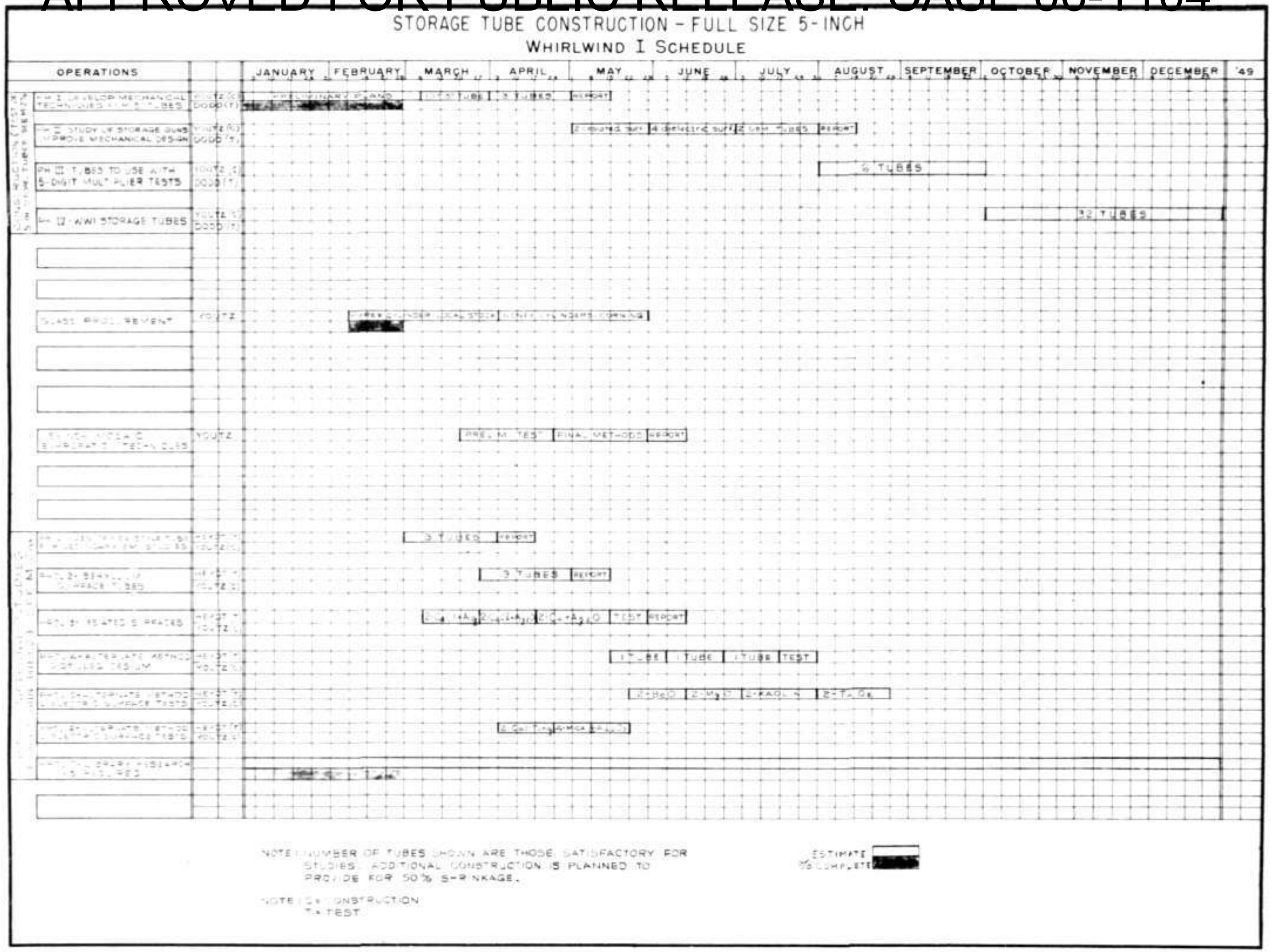
SUMMARY - WHIRLWIND I SCHEDULES



SUMMARY – WHIRLWIND I SCHEDULES CONT.




B – REGISTER
WHIRLWIND I SCHEDULE
OPERATIONS
MIT
S
JANUARY
FEBRUARY
MARCH
APRIL
MAY
JUNE
JULY
AUGUST
SEPTEMBER
OCTOBER
NOVEMBER
DECEMBER
'49
Circuit Schematic
Drawings + Approval
Layout
Approve + Change
Production Drawings
Approve + Change
Procurement
Prototype
Construction
Electronic Test
Approve + Change
Construct + Test 18 Units
SYLVANIA VACATION
Estimate
% Complete


STORAGE TUBE CONSTRUCTION - FULL SIZE 5-INCH
WHIRLWIND I SCHEDULE
OPERATIONS
JANUARY
FEBRUARY
MARCH
APRIL
MAY
JUNE
JULY
AUGUST
SEPTEMBER
OCTOBER
NOVEMBER
DECEMBER
'49
PH III TUBES TO USE WITH 5-DIGIT MULTIPLIER TESTS
PH IV WWI STORAGE TUBES
6 TUBES
32 TUBES
3 TUBES
REPORT
PRE. M. TEST
FINAL METHODS
1 TUBE
TEST
NOTE: NUMBER OF TUBES SHOWN ARE THOSE SATISFACTORY FOR STUDIES. ADDITIONAL CONSTRUCTION IS PLANNED TO PROVIDE FOR 50% SHRINKAGE.
NOTE: (C) = CONSTRUCTION
T = TEST
ESTIMATE
% COMPLETE

The two time schedules on pages 6 and 7 are examples of the individual schedules from which the summary schedule is compiled.

Check marks show the principal division of remaining work between MIT and Sylvania.

THE EFFECTS ON COMPUTING SPEED OF ACCESS TIME, PULSE REPETITION FREQUENCY, AND REGISTER LENGTH

The computing speed of WWI is a function of storage access time, pulse repetition frequency of the two clock-pulse supplies, and register length.

For any given problem the total computing time is determined by the numbers of the different operations to be carried out, since such diverse operations as addition and division require differing times. In general terms, the only concise ways of representing the speed of the computer are (1) to estimate its average speed for an assumed normal distribution of operations or (2) to count onlv a certain operation which consumes the bulk of the time. In WWI all operations are of comparable although differing durations. The average time seems to be the best criterion, the approximate time required for a given problem being obtained by multiplying this average by the total number of operations or orders to be carried out. The discussion below considers first the basic time requirements common to all operations and then adds to this the extra time for other operations multiplied by the ratio of their usual occurrence.

Storage access time has the greatest effect on computing speed. Two references to storage must be made for each operation, one for extracting the order, the other as part of carrying out this order. The time required to operate storage thus represents a minimum below which it is not possible to reduce an operation time.

In WWI a sequence of eight low-frequency time pulses generate the normal setup and arithmetic-control functions for each operation. In order to speed up the computer, six of these pulses overlap the storage operation.

Therefore, unless storage access time is reduced below three low-frequency pulse intervals, which is unlikelv, low-frequency prf has an effect on onlv two pulse times per operation.

High-frequency clock pulses are used in the arithmetic element during multiplication and shifting operations. These operations include the normal two storage-access intervals plus two low-frequency pulse intervals plus the high-frequency part of the operation. Actually the frequency of occurrence of the various operations is such that only multiplications and so-called normal orders (additions, transfers, etc., requiring no high-frequency pulses) are important. Divisions and shifts do not appreciably affect average computing time except in unusual problems. Furthermore, examination of sample problems shows that approximately one in every ten operations is a multiplication. Thus the effect of high-frequency prf is only on the high-frequency part of multiplication beyond the normal setup time. This effect must be divided by ten in order to average it over all operations.

The time required for the high-frequency part of multiplications is a linear function of register length, since the number of successive additions is equal to the number of digits. When the register length is made large enough (40 digits) to hold two complete orders in one word, the storage operation time is effectively reduced since there are then an average of only 1-1/2 storage references per operation. Because of this, the computing time for the 40-digit register length is in general lower than for the shorter register lengths.

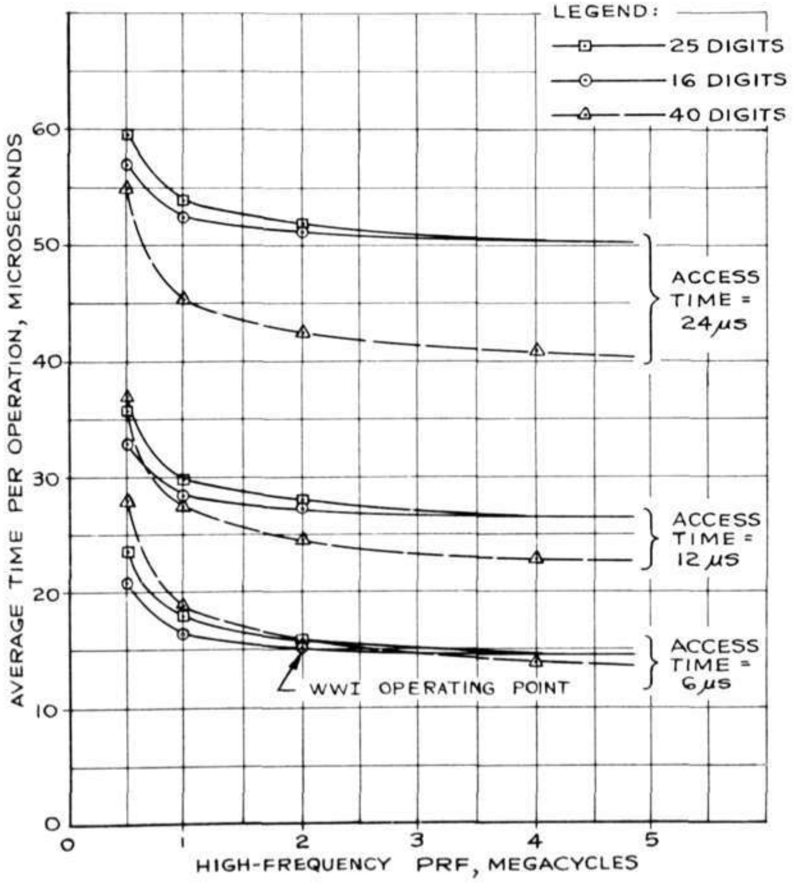
The accompanying curves show the average time per operation plotted against high-frequency prf. Low-frequency prf is taken as 1 megacycle for high-frequency prf's above 1 megacycle and as equal to high-frequency prf below 1 megacycle. This assumption causes a break in the curves at 1 megacycle.

Three sets of curves are given, corresponding to storage access times of 6, 12, and 24 microseconds. This access time includes setting storage switches, establishing deflection voltages, tube operation including checking and restoring, and transfer of stored information. Times for reading and writing are assumed equal.

For each access time three curves are given corresponding to register lengths of 16 binary digits (WWI), 25 binary digits (a probable length for control and simulation computers), and 40 binary digits (a useful length for scientific calculation).

Note that storage access time has an overwhelming effect on computing speed. The effect of prf above 1 megacycle is essentially unimportant unless the storage access time can be made very short. Below 1 megacycle, prf becomes increasingly important. A point is marked on the curve for the operating conditions of WWI when a 6-microsecond storage access has been achieved. WWI prf has been made higher than would otherwise be jus-

COMPUTING SPEED vs. HIGH-FREQUENCY
PULSE-REPETITION FREQUENCY
FOR VARIOUS ACCESS TIMES AND REGISTER LENGTHS



tified because it was designed as a prototype of other computers that may have longer register lengths and that may be used for the solution of problems involving a larger proportion of multiplications. Furthermore, the techniques for using higher frequencies in the arithmetic element may in the future be extended to other parts of the computer as justified by increases in storage speed.

CODING FOR SIMULATION

The use of a high-speed computer for simulation presents problems to the machine designer and operator that are in many ways radically different from the problems involved in the use of such a machine for scientific calculation.

Simulation is the substitution of a computational process for some real physical process. Simulation constitutes a means for setting up in the laboratory a working model of a complex process. This working model can be used for studying the behavior of the process, developing equipment for controlling the process, and training human operators to control the process. Simulation problems therefore exhibit the following characteristics:

1. Since the simulator operates in combination with human beings or with real physical equipment, it must operate on a real or 1:1 time scale. Computing speed must therefore be high. In a simulated military engagement involving ships, submarines, and airplanes, for example, a fast computer is needed for presentation of useful information. Further speed increase can be used either to obtain a more detailed representation of the actions of each target or to increase the number of targets which can be considered. There seems little doubt that all the computing speed which can foreseeably be obtained can be used effectively.

2. The mathematical problems involved are not serious despite the enormous amount of computation required. In general, simulation requires the repetition of simple sequences which are sufficient only to give a reasonable representation of the process being solved. The sequences may range from a few dozen operations for a ship maneuver to a few thousand for a multi-engined aircraft in flight. The time constants involved are usually such that solutions must be given at least every few seconds and in many cases several times a second if a realistic representation is to be obtained.

Furthermore, these solutions do not represent merely the intervals in a lengthy computation but rather the end results themselves. Since the computer is simulating a process, its solutions are by definition the physical conditions at each step so long as the representations are reasonable. Long-time solution stability is of reduced importance because at the end of each solution, corrections or changes in the inputs are provided by the human or mechanical controllers. In other words, there is no reason to require the computer representation to predict the actual process over long periods of time and many solution intervals as it must in the more usual prediction-type of computing. The representation over short periods of time should, however, be good.

Since the computing sequences are essentially short, roundoff and trucation errors are of relatively small importance, and necessary register length is determined almost entirely by the required sensitivity of the variables. The register length can be much shorter than that required for scientific calculation. Instead of 10 decimal digits, 5 will probably be sufficient, although an increase to 6 or 7 may be desirable. Where some few particularly sensitive quantities must be used, two registers may be employed. It is expected that the 16 binary digits, with occasional doubling of registers, of the prototype WWI will be adequate for most problems. Later models built particularly for simulation may have their register length increased to about 25 binary digits. It is important to keep the register length short since the amount of equipment in a computer of the WWI type is almost linearly dependent on the number of digits.

3. Storage capacity should be high since it may be necessary to store many variables in order to describe the condition of each of the many elements of a problem. It may also be necessary to store large amounts of empirical data in the form of functions of several variables in order to describe the dynamic characteristics of certain elements. Since the computer must operate in real time, and since subsidiary or intermediate-speed memories are relatively slow, it is important that all information needed by the machine be available to it in its high-speed memory. Effective reference to a subsidiary memory can be made only if a drastic change of conditions is required, a change which will obscure the resulting loss of solutions.

The net requirements may be summarized as follows:

1. Computing speeds must be high because of the need for real-time solution.
2. Register length may be short because the short computing sequences used reduce the

effect of roundoff and truncation errors.

3. High-speed storage capacity must be large in order to give the computer rapid access to all pertinent information.

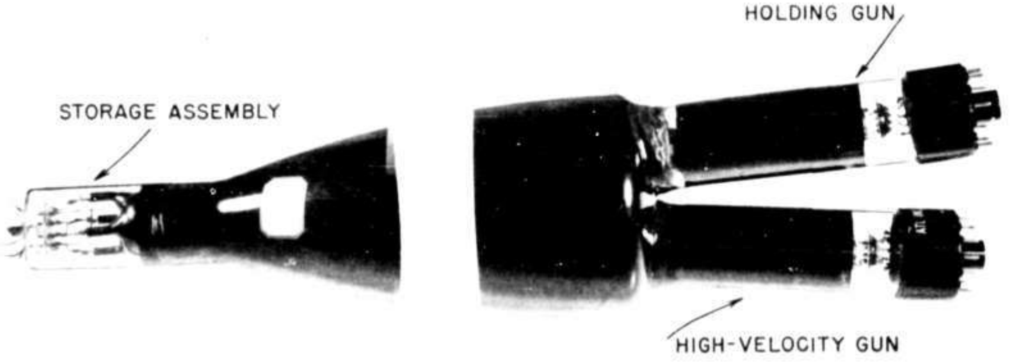
Although WWI was designed primarily as a computer prototype, investigations to date have shown that its design characteristics of 20,000 multiplications per second, 16-binary-digit register length, and 2048 storage registers are in good balance for simulation and control purposes.

STORAGE

Tubes

The electrostatic storage tubes being developed for the Whirlwind computers use a high-velocity well-focussed beam for storing digits as spots of positive or negative charges on a storage surface, and a low-velocity diffuse beam spraying the surface to maintain the stored charges. A metal backing plate (or signal plate) picks up the signal current by capacitive coupling to the storage surface. Research tubes were constructed for studying storage phenomena on different types of storage surfaces. These tubes for research studies were constructed in modified cathode-ray tube envelopes with 3/4-inch diameter storage surfaces as shown in the accompanying photograph. This small storage assembly was used because it is easily constructed and because its low capacitance allows the use of available test equipment.

Storage tubes for satisfactory operation with WWI will require 5-inch diameter storage surfaces. Construction problems and techniques to produce these large tubes are being investigated. One of the first problems encountered in using these large surfaces is the demand for a uniformly dense holding beam with a very high total current. Standard guns do not produce such a diffuse beam, so that they must be modified. Three research tubes have been built to test proposed modifications on a standard 5UP gun. The following basic changes in gun structure were made: First, the electrode apertures were enlarged to give a diffuse high-current beam. Second, the connection to the accelerating grid was brought out so that it could be operated at a high potential, yielding high cathode emission. Third, the control grid of the gun in one tube was replaced by a wire mesh to give larger exposed cathode area. Results of the testing of these tubes indicate that deflection plates cast shadows and must either be moved from the electron stream or deleted. Greatly increased total currents of about 500 microamperes were obtained. More electron guns will be modified and tested in research tubes to obtain a holding gun satisfactory for experimental work on 5-inch tubes. New gun designs may be required eventually but are not necessary for present work.



RESEARCH TUBE FOR THE STUDY
OF STORAGE PHENOMENA

The 5-inch tube program also requires new techniques for construction of the storage assembly. The large-diameter screens must be kept under tension during construction, processing, and operation to prevent heating cycles, electrostatic forces, and other disturbing factors from distorting the flat screen surface. Components for the first experimental assembly have been constructed. If the completed assembly is satisfactory, it will be used in the first 5-inch tube. This tube will use the best holding gun available about the middle of March; construction and processing will be completed by the end of March.

Read-Out Circuits

In the process of "reading out" a binary digit from the electrostatic storage tube, the signal pulse is superimposed on a switching pulse whose amplitude greatly exceeds that of the desired signal. The switching pulse is required to change the potential of the storage tube signal plate during the reading operation. The read-out circuit must be able to pass the signal pulse without attenuation, but must suppress the transients caused by the switching pulse. The problem is complicated by the fact that it must be possible to complete each reading operation within a few microseconds.

Several circuits have been proposed which may accomplish this task with a maximum of simplicity and a minimum number of tubes, and an experimental investigation of these circuits has been undertaken recently by the Project. No results can be given as yet, but the general methods which are being investigated can be outlined briefly.

It may be possible to construct a read-out circuit which will pass the signal pulse, but which will resolve the rectangular switching pulse into a pair of narrow pulses which have much smaller amplitude than the switching pulse and which coincide in time with its leading and trailing edges. Two methods to meet these requirements are under consideration at present. One involves the use of an electronic two-position impedance-switching device. The other utilizes a three-winding transformer, one of whose secondary windings couples the switching pulse to the signal plate while the other secondary provides a bucking voltage to oppose the switching pulse at the input to a delay-line differentiating circuit. The delay line should resolve the reduced switching pulse into a pair of small pulses. With the signal pulse midway between these two pulses, it could be selected by an electronic gating system.

On the other hand, it may be possible to devise a coupling circuit which will not pass the switching pulse at all, but which will pass the signal pulse. A transformer-coupled read-out circuit has been suggested in which the switching pulse would drive the whole primary winding of the transformer positive during the switching interval. The signal pulse would occur during this interval and would be coupled to the output winding of the transformer.

Deflection Circuits

Each of the electrostatic storage tubes used as a memory element in the Whirlwind computers is to have 1024 available storage positions. The position to be used for any storage operation will be specified in the program order which calls for that operation, the information being supplied to the storage-control circuits as a binary number in pulse-coded form. A group of "deflection circuits" in the storage control system will convert the pulse-coded number into two potential differences whose magnitudes correspond to the magnitude of the input number. These potential differences will then be applied to the deflection plates of the electron guns of all storage tubes in the system, and will thus control the position on the storage surface at which the storage operation is performed.

Following investigations into the deflection-circuit design problem carried out during the past year, it has been decided to construct a preliminary model of the deflection circuits which will be used with the 5-inch electrostatic storage tubes. While it is expected that the design of this preliminary model will require additional refinement for use in WWI, current specifications for WWI electrical and mechanical design have been used as a guide in preparing circuit schematics and mechanical layouts.

The circuit chosen for the preliminary model appears to be the one most suitable for use with large banks of electrostatic storage tubes of the type now being developed by this Project. Conversion of the pulse-coded number into an electrical magnitude is accomplished by causing each pulse of the input number to turn on a current source. The current sources are weighted in accordance with the code used in representing numbers, and their outputs are mixed in a low resistance. A voltage proportional to the sum of the currents then appears across the resistance and is applied to the input of an electronic amplifier whose output is of sufficient amplitude to produce the desired deflection of the beams of the connected storage tubes.

Two staff members are currently assigned to full-time work on the development of deflection circuits. A time schedule has been prepared calling for completion of the preliminary model of the deflection circuits by May, 1948, and for completion of tests on this model by June, 1948. Design of the unit has been completed and construction of the first of its component panels is currently in progress. Design tests will be performed on this panel before construction of the rest of the unit is begun.

POWER SUPPLIES

In March, 1946, a central system was planned to distribute power in a uniform manner to all laboratories and work benches used by the electronic staff and technicians.

Most of the supplies consist of two variacs on a common shaft followed by two plate transformers. These plate transformers have six matched secondaries, followed by pairs of mercury rectifiers. It is possible to connect the transformer secondaries in various parallel and series combinations to give a wide range of output voltages, and the final settings can be made with the variac. The output voltage is filtered by identical 2-stage LC filters employing plug-in electrolytic capacitors and conventional iron-core chokes. These filters reduce the ripple to less than 0.1 volt.

In addition, each supply has its own time-delay relay, meters, bleeder resistor, and switch, providing flexibility in use and servicing.

The higher voltage supplies are unregulated but have low output impedance and satisfactory output regulation where the a-c line stability is good. The low-voltage supplies are regulated by means of a saturable-core reactor which varies the input voltage to selenium rectifiers.

Central supplies are used for two reasons:

1) In 1946 when the change was made, a staff of ten men were using over 90 individual supplies. These supplies were bulky and troublesome.
2) The use of individual supplies permitted too much variation in voltages used in experimental and research equipment. Thus, it was difficult to judge test results, evaluate designs, and coordinate development.

The supplies, except for bias voltages, are unregulated and deliver 10 amperes of d-c power into a central bus system. At eight points in the building, distribution boxes are attached to the bus lines. Each of these boxes incorporates an instantaneous (1 millisecond) circuit breaker for protection of personnel and equipment. The output sides of the circuit breakers feed 6 parallel-connected 12-pin Jones receptacles. Each laboratory bench has a 10-conductor cable and plug for attachment to these distribution boxes. At each bench, this cable is brought into a distribution box containing four 12-pin Jones receptacles and a 10-pole switch for disconnecting all d-c power. A 20-ampere, 6.3-volt filament transformer is attached to each bench and its output connected to terminals on the Jones receptacles. A stock of 12-conductor cables with Jones plugs, as well as local control boxes and similar accessories, are available for quick connection of power to equipment.

Although other voltages were available during evolution of the central system, standard voltages now available are those used in WWI as listed below.

Both transient and steady-state changes in the primary a-c power cause trouble, and a synchronous condenser with series reactors is being installed to provide voltage control.

STANDARD VOLTAGES AND TUBES FOR WWI

Voltages

During the initial stages of WWI development, circuits were designed to perform the functions outlined by the block diagrams with relatively little consideration of power-supply requirements. However, integration of many electronic elements into a working computer can best be done if the problems of power supply and distribution are simplified as much as possible by use of a minimum number of different voltage levels.

While the voltages that have been adopted were determined largely by the requirements of circuits already designed, several slight modifications in operating potentials were made in these circuits whenever it was apparent that use of the standard voltage would not impair operation.

Power supplies are being designed to provide the eight d-c voltage levels chosen as standard for WWI: -150, -30, -15, +90, +120, +150, +250, +500 volts. In addition, a 6.3-volt a-c source will be provided for the vacuum-tube cathode heaters.

These voltages are already available in the laboratory, where final tests on WWI circuits are in progress. The range is sufficient to provide adequate flexibility for the design of new circuits.

Tubes

Exclusive of electrostatic storage tubes, Whirlwind I will contain about 3500 vacuum tubes of types which were chosen on the basis of performance characteristics and available information on reliability. The following table is a breakdown of requirements:

Tube Type	Number Required
7AK7	1300
6AG7	1100
5692	550
6Y6	200
829, 6L6, 6AK5, etc.	350
Total	3500

The 7AK7, developed for Project Whirlwind by Sylvania Electric Products Inc., is a pentode whose similar high-transconductance suppressor-grid and control-grid characteristics are ideally suited for use in gate circuits, from which an output pulse is desired only upon simultaneous excitation of two grids of the so-called gate tube.

WWI flip-flops use pairs of 6AG7 tubes, one of which is conducting at all times. The sharp cutoff and high transconductance of this high-performance pentode type meet the requirements for fast switching of the flip-flop from one to the other of its stable states. Computing speed is highly dependent upon the time required to complete this switching action.

The condition of each flip-flop, and therefore its binary-digit content, is continuously indicated during steady-state operation by a pair of neon lights. These lights are each excited by one half of a 5692 (a "ruggedized" 6SN7) dual triode whose grids are coupled to the plate terminals of the flip-flop 6AG7's.

High pulse currents such as are required for applying adequate voltage signals to low-impedance transmission lines are best provided by beam-power tubes like the 6Y6, 829, and 6L6. The most common Whirlwind "line-driving" circuit uses a 6Y6 tube with a 5:1 pulse transformer in its plate circuit for maximum power transfer to the terminated coaxial cable used for distributing pulses throughout the computer.

Other tube types, such as the 6AK5 miniature, are used in miscellaneous applications when appropriate.

APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were issued during February.

No.	Title	No. of Pages	No. of Dwgs.	Date	Author
E-95	Standard Circuits, Gate Generator GG-1	2	1	1-28	J. A. O'Brien
E-96	Ground Circuits for WWI	1	2	1-28	D. R. Brown
E-97	Storage Tubes Requirements for WWI	3	3	2-3	S. H. Dodd
E-98	A capacitively coupled Flip-flop (Abstract, Thesis Report)	2	-	1-16	A. B. Horton
E-99	Test Equipment, Standard Tube Test Panel	1	-	2-16	N. H. Taylor
E-100	Life Rack for Sample Storage Surfaces	2	-	2-17	H. Heydt
E-101	Coupling Capacitors in Basic Circuits	1	-	2-17	C. W. Watt
M-206	Numerical Solution of Systems of Simultaneous Linear Algebraic Equations by Elimination Methods	17	-	1-8	E. Reich
M-218	Production Quantities of WWI Units	1	-	1-23	H. Fahnestock
M-219	WWI Drawing Procedure (Note to Sylvania)	1	-	1-23	H. Fahnestock
M-222	D-C Voltages Required for WWI	1	-	1-27	C. W. Watt
M-223	Air-conditioning for WWI	2	-	1-29	J. Proctor
M-226	Floor Loading for WWI Computer Room	2	-	2-2	R. E. Hunt
M-228	Whirlwind I Preliminary Time Schedule	1	-	2-3	H. Fahnestock
M-229	Meetings of Electronics Group January 26 and 28th.	1	-	1-30	J. A. O'Brien
M-230	Notes on Aquadag	3	-	2-4	F. Caswell
M-231	Eastman Conference of December 23 and January 20 and 21.	5	-	2-4	H. R. Boyd
M-232	Measurement of 7AK7 Characteristics at Emporium February 2 and 3, 1948	2	-	2-6	D. R. Brown
M-233	Meeting to Discuss Storage Tube Output Systems	2	-	2-5	C. Campling
M-235	Vacuum Tube Life Tests	2	-	2-9	J. Forrester
M-236	Flip-flop Storage Arrangement	1	-	2-9	H. Fahnestock
M-237	Bi-Weekly Report, Part I Feb. 6	9	-	2-6	
M-238	Bi-Weekly Report, Part II Feb. 6	15	-	2-6	
M-239	Order of Combination of Arithmetical Operations for Minimum Round-off Error	4	-	2-13	E. Reich
M-240	A New Order for Finding Characteristics	1	-	2-13	P. Franklin
M-241	Comments on Program Register Demonstration Panel	5	-	2-17	H. Fahnestock
M-242	Twin Triodes	1	-	2-17	H. Fahnestock
M-244	Project W. W. Seminar Schedule Feb. 6 - Mar. 10	2	-	2-18	R. R. Everett
M-245	Bi-Weekly Report, Part I Feb. 20	11	-	2-20	
M-246	Bi-Weekly Report, Part II Feb. 20	18	-	2-20	

Translations and Transcriptions

No.	Title	No. of Pages	No. of Dwgs.	Date	Author
M-172	The Motion of the Ionic Lattices of Dielectrics in Extreme Electric Field Intensities: A. Guntherschulze and Hans Betz, ZEITSCHRIFT FUR PHYSIK, Vol. 92, 1934, pp. 367-374	7	-	12-1	M. Florencourt
M-224	A Method of Direct Measurement of Secondary Electron Emission at Insulators: W. Heimann and K. Geyer, ELEKTRISCHE NACHRICHTEN - TECHNIK 17:1:1-5 (1940)	6	-	1-29	M. Florencourt