Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A SEQUENTIAL-ACCESS THREE-MICROSECOND CORE MEMORY

To: R. R. Everett, W. B. Davenport, Jr., and F. A. Rodgers

From: R. L. Best and T. H. Meisling

Date: 8 March 1956

Approved: DRB
D. R. Brown

Abstract: A proposed core memory is described that has sequential access to 256 registers (word storage locations), can read out a new word every 3 microsecond and has word length of 58 bits. A read-rewrite cycle for a given storage location requires 6 microseconds; the rewrite (or write), is accomplished during the 3 microsecond period that the next storage location is being read. Direct storage-location selection provides a 3-to-1 selection ratio. Small, low-coercive-force cores are used (0.047 in. O.D., F398, DCL-5-19S-1). Since currents required are small, transistors can be used instead of tubes.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Introduction

A core memory using register selection a 3:1 write has been described.[1] The unusual feature of the memory to be described here is that in addition to register selection and 3:1 write, reading is done in any one register while writing is done in the register in which reading has just been completed. Two cores per bit are used to present a more constant load to the memory drivers and to give a better read signal (a "one" always appears as one polarity output pulse while a "zero" always has the opposite polarity).

Principle of Operation

Figure 1 shows 4 registers (word storage locations) and 2 digits (places) of the memory. The selection drive lines have 3-μsec unipolarity current pulses applied in a sequential manner. Figure 2 shows the selection current waveforms (idealized as to rise and fall times) in selection windings "i-2" through "i+1". Figure 1 shows how the full selection current in selection line "i" goes through all the cores of register "k", while a fraction of it (determined by the values of R_a, R_b, and the core back voltages) goes through cores in register "k-1" in the opposite direction. Figure 3 shows the net (idealized) currents in registers "k-2" through "k+1" caused by the selection currents "1-2" through "i+2".

A current of unity will switch one of these cores in 2 μsec with a small output voltage, while a current of 8/3 will switch a core in less than ½ μsec (with a much larger output voltage). "Digit drive" in Figure 4 shows a typical digit pattern of write information i.e., a time sequence of bits written into the particular place, of 00011. This current is added to the net selection currents in the "B" cores and subtracted from the net selection currents in the "A" cores in accordance with Figure 1. Figure 4 shows the resultant net current for each core in the core pairs "k-2" through "k+1". In register "k", reading is being done during time interval "C" (both "A_k" and "B_k" have the large read current, and are left in the cleared state. Writing is done during "D", the next time interval, when core "A_k" has a current of -1/3 and "B_k" has a current of -1. Since a current of unity will switch a core and a current of 1/3 will not, core "B_k" gets switched to the "set" state during "D" and "A_k" is left cleared. Only one core of any pair will be switched during writing, so that only one core of any pair can be switched during reading. If an "A" core is switched during reading a negative pulse appears at the sense amplifier input, and if a "B" core is switched during reading a positive pulse appears at the sense amplifier. Figure 4 shows that registers "k-2" and "k-1" are having "zeros" written in them ("A" cores are being set) while registers "k" and "k-1" are having "ones" written ("B" cores are set).

---

[1] "A Linear Selection Magnetic Memory Using an Anti-Coincident Current Switch", by K. H. Olsen, M-2110.

Figure 5 shows switching time and output voltage vs ampere-turns for a core of the type that is proposed for this use. The body is DCL-5-19S-1, and the size is F398 (0.027 in. I.D., 0.047 in. O.D.) From these data, a current of "unity" would be made 110 ma; the selection current would be 8/3 times this or 296 ma and the digit current 1/3 times 110 or 36.7 ma. The net read current would be 7/3 or 9/3 times 110, or 256 or 330 ma. Figure 5 shows the output voltages for these currents to be 85 and 150 mv, and the switching times to be 0.55 and 0.4 μsec. The output voltage for a core being written into with a unity current (110 ma) would be 15 mv, and the switching time 2 μsec.

The above data were used in Figure 6, which shows the contribution to the sense amplifier input from each core. Figure 7 shows the total digit winding output. In these figures the solid lines represent the waveform that would be generated if "ones" were being read out, while the dotted lines represent the waveform if "zeros" were being read. This net waveform clearly shows that "zeros" are being written during intervals "A", "B", and "C" and that "ones" are being written during intervals "D" and "E". A study of the figures will show how the two amplitudes of read pulses are caused by the addition (or subtraction) of the digit and selection currents and voltages.

Notice that the information read out of register "k" occurs during the first half microsecond of time interval "C". During the remaining 2.5 μsec of this interval any computation necessary may be done on this information. At the beginning of time interval "D" the information to be written in register "k" is fed to the memory input register (MIR) and the new word is read in to register "k" during the following time interval, "D". During the first half microsecond of any time interval the voltage input to the sense amplifier has a polarity dependent only the information being read out, simplifying the sense amplifier problem. The digit current may be left on continously; that is, each digit driver is direct coupled to its corresponding flip flop in the MIR.

Register Selection Switch

Figure 8 shows a method of selecting the 256 loads (selection drive lines) that requires only 32 high-power transistors, and 256 diodes capable of handling the selection current. Diodes are available to handle currents of 296 ma, but such diodes in general do not have good reverse-recovery times. A study of Figure 8 will show that no diode in the same row or column as the selected diode has back voltage applied. Therefore, it is possible to arrange the sequencing of the "u" and "v" input lines so that no diode has back voltage applied to it during the 3 μsec interval following the interval during which it conducts. All that is necessary to accomplish this is to insure that the "u" and "v" addresses do not change at the same time. Figure 8 shows an acceptable order of selectiong diodes (and loads) which satisfies this requirement (the loads are to be selected in the order in which they are numbered), and Figure 9 shows how this is accomplished. It is assumed that the memory address register is connected as a binary counter. Addresses

"u_0" and "u_{15}" are interchanged when FF3 containes a "one", and are not interchanged when FF3 contains a "zero". The register must be connected as a conventional counter since the address is contains is to be used in other places in the computer for which this memory was conceived.

R. L. Best

R. L. Best

Torben Meisling

T. H. Meisling

RLB:lj

Attachments:

SA-65543 - Figure 1
SA-65544 - " 2 and 3
SA-65545 - " 4
SA-48734 - " 5
SA-65546 - " 6 and 7
SA-65547 - " 8
SA-65548 - " 9

Distribution List:

*Axelbank, M.
*Barrett, B.
*Bajemore, T.
*Bivans, E.
*Clark D.
*Davenport, W.
*Dineen, G.
*Dood, S.
*Everett, R.
*Forrester, J.
*Fortier, O.
*McDonald, W.
*Nelson, B.
*Papian, W.
*Rodgers, F.
*Taylor, N.
*Fadiman, J.
*Gurley, B.
*Highleyman, W.
*Konkle, K
*Peterson, M.
Callahan, R.
Flanagan, M.
Hingston, A.
McCusker, J.
Paddock, R.
Sutro, L.
*Goodenough, J.
*Eckl, D.
*Mitchell, J.
*Clark, W.
*Olsen, K.
*Meisling, T.
*Best, R.
*Corderman, C.
*Buck, D.
*Bradspies, S.
*Davidson, G.
*Ellis, D.
*Guditz, E.
*Sarles, F.

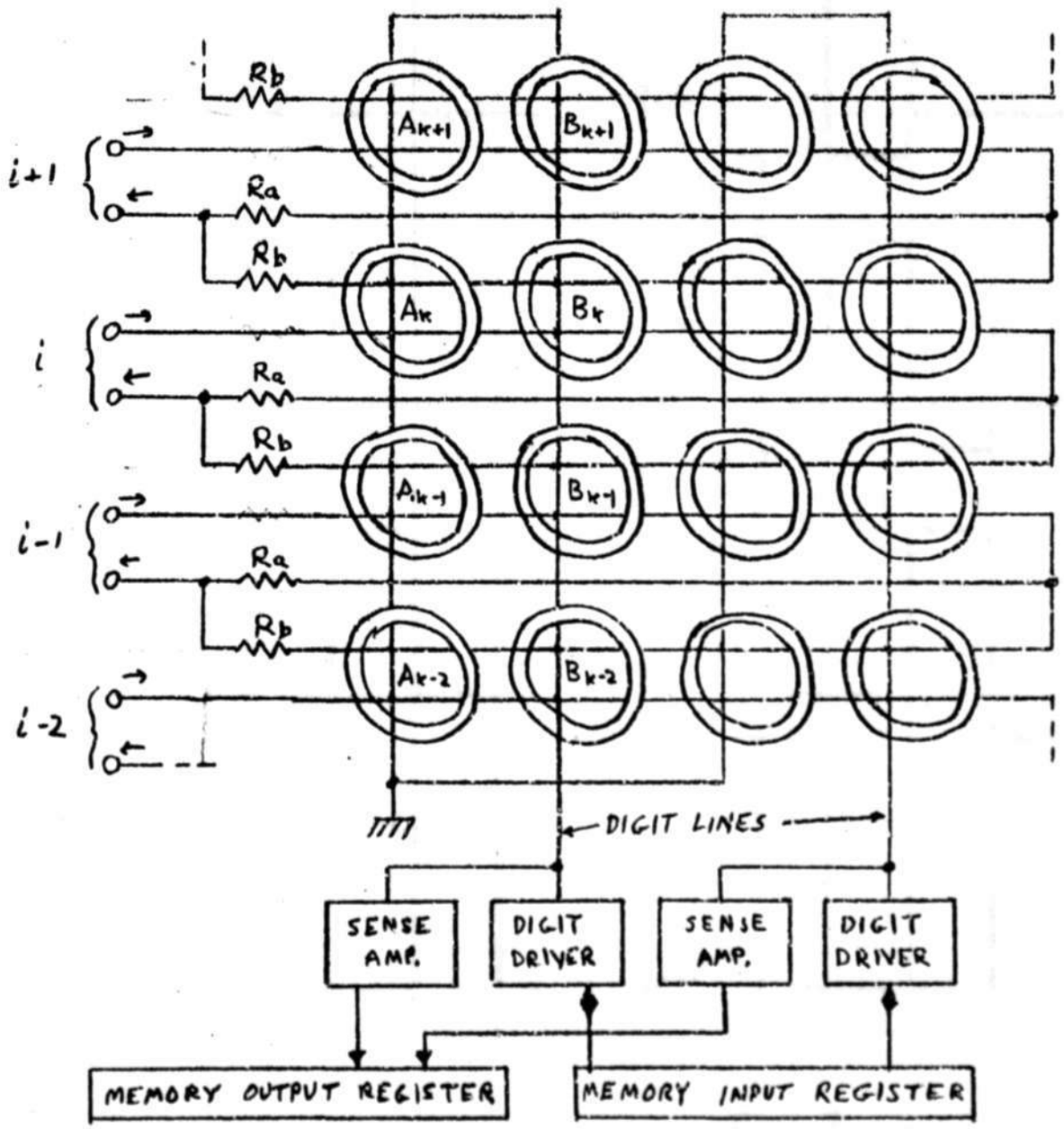


FIG. 1 4 REGISTERS AND 2 DIGITS OF MEMORY SHOWING SELECTION AND DIGIT LINES

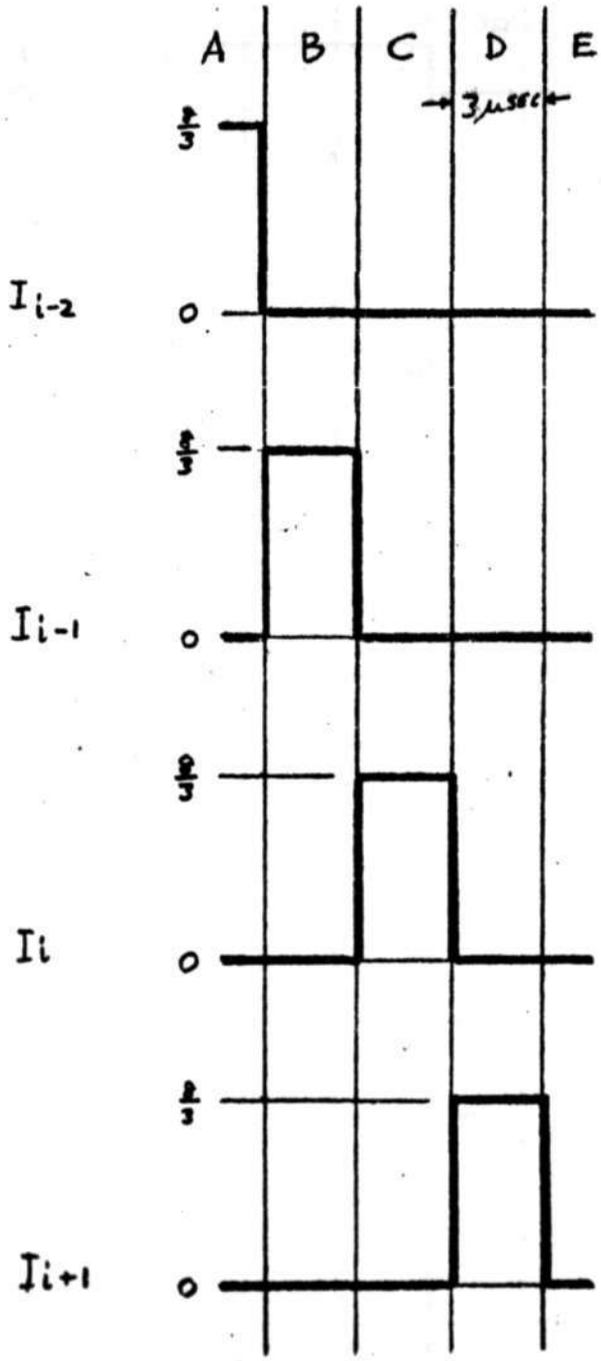


FIG. 2 SELECTION DRIVE LINE CURRENTS, IDEALIZED WAVEFORMS

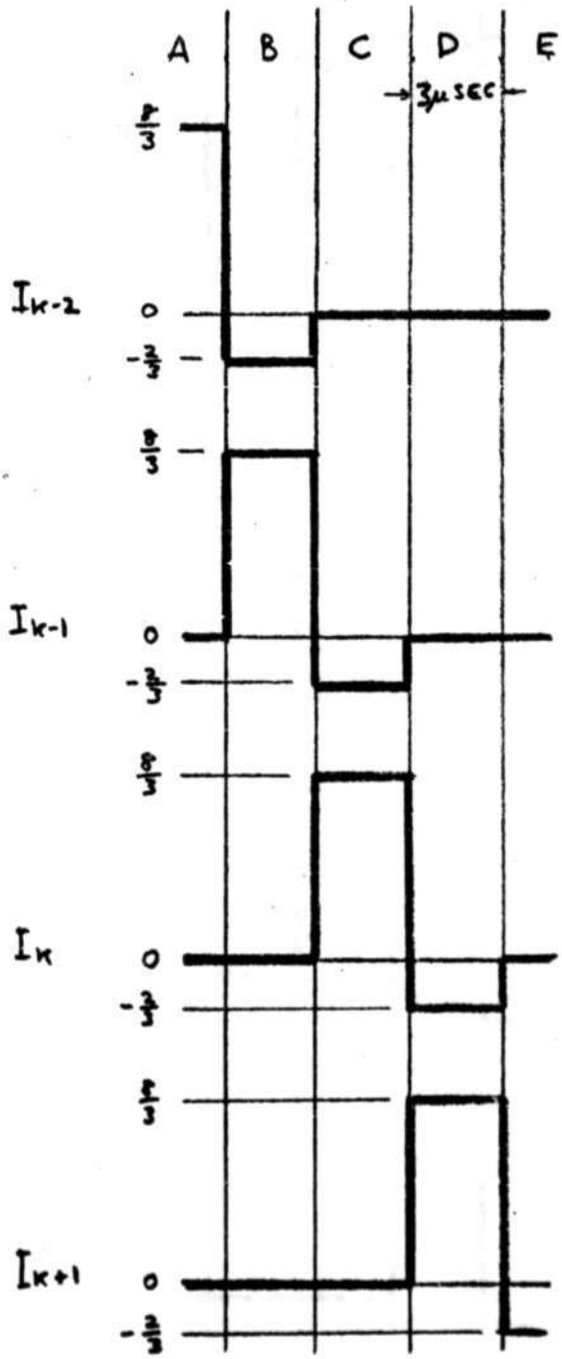


FIG. 3 NET SELECTION CURRENT IN EACH REGISTER

A CURRENT OF UNITY WILL SWITCH A CORE IN 2 μSEC.

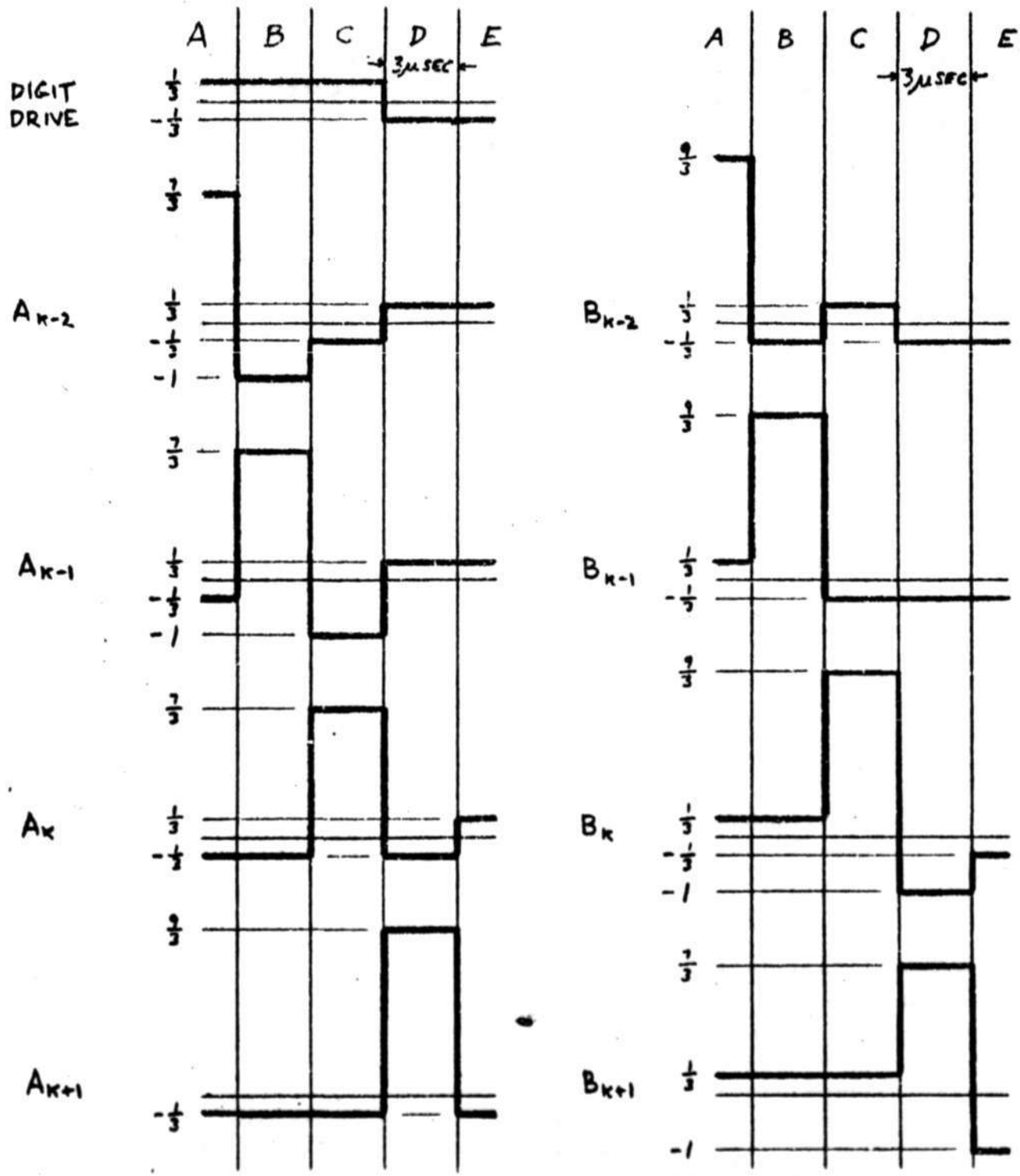
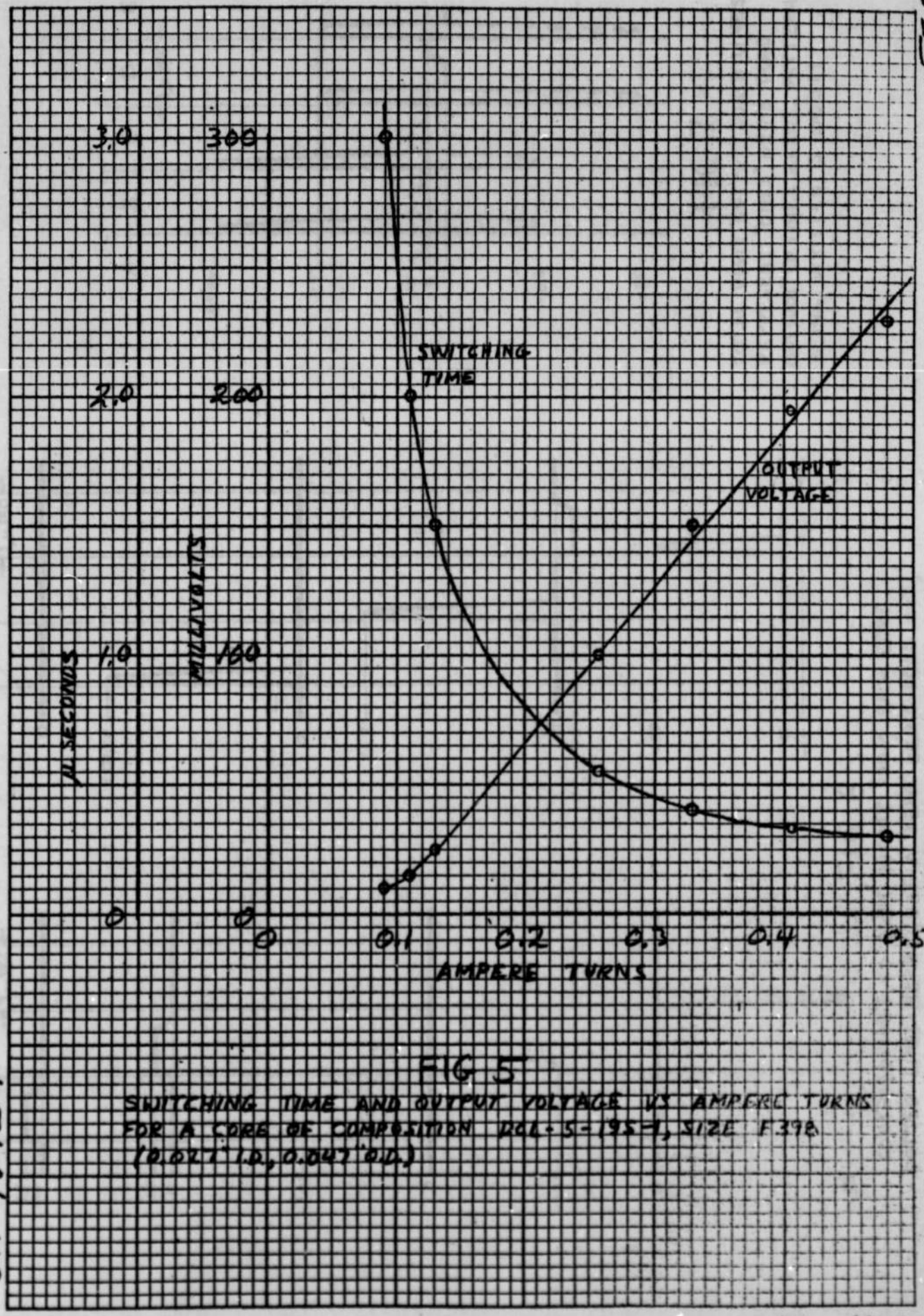


FIG. 4 NET SELECTION CURRENT IN EACH CORE (NET SELECTION CURRENT PLUS DIGIT DRIVE). A CURRENT OF UNITY WILL SWITCH A CORE IN 2 μ SEC. PATTERN BEING WRITTEN IS 00011.

SA-48734



SA-48734

FIG 5

SWITCHING TIME AND OUTPUT VOLTAGE VS AMPERE TURNS FOR A CORE OF COMPOSITION DCL-5-195-1, SIZE F398 (0.021" I.D., 0.047" O.D.)

SA-48734

SA-48734

SA-65546

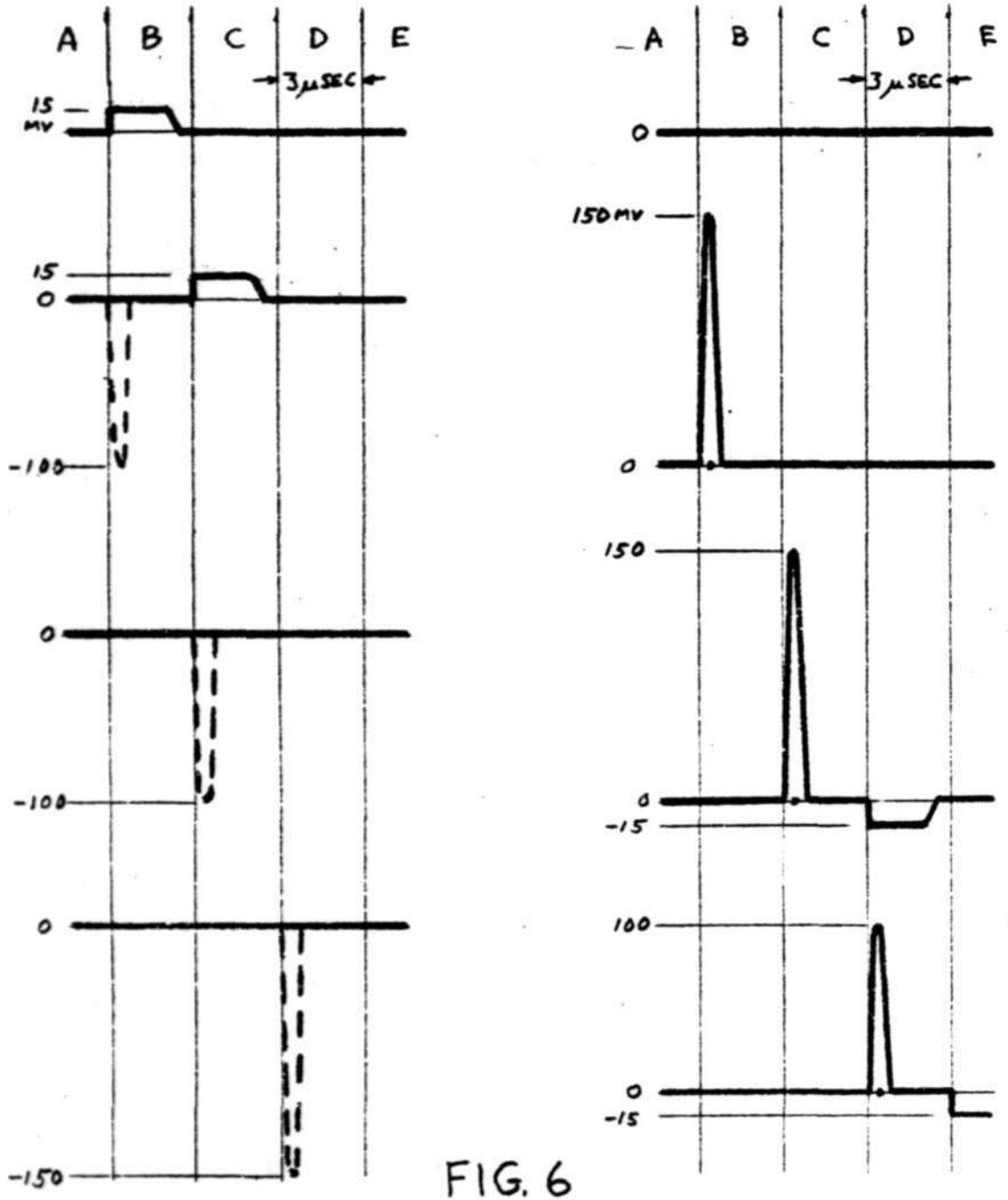


FIG. 6

CONTRIBUTIONS TO DIGIT OUTPUT FROM EACH CORE. DOTTED LINES REPRESENT A "ZERO" BEING READ OUT; SOLID LINES REPRESENT A "ONE" BEING READ OUT.

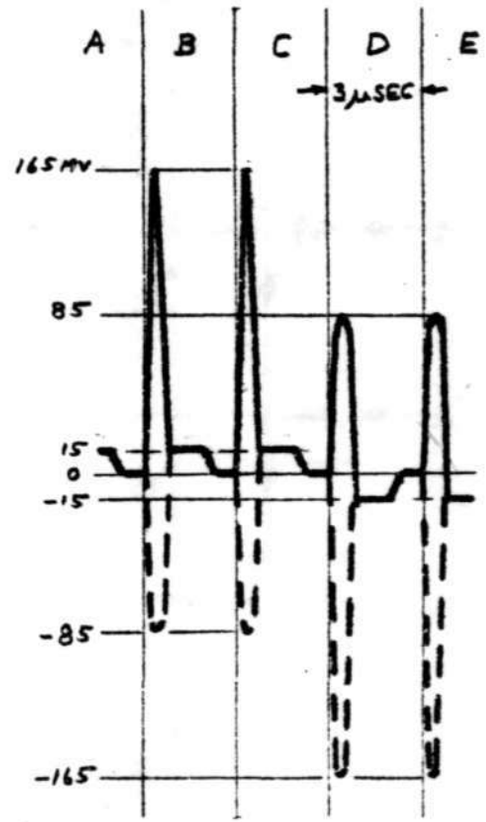


FIG. 7

TOTAL DIGIT OUTPUT. SOLID LINES REPRESENT "ONES" BEING READ OUT; DOTTED LINES ZEROS. PATTERN BEING WRITTEN IS 00011

SA-65546

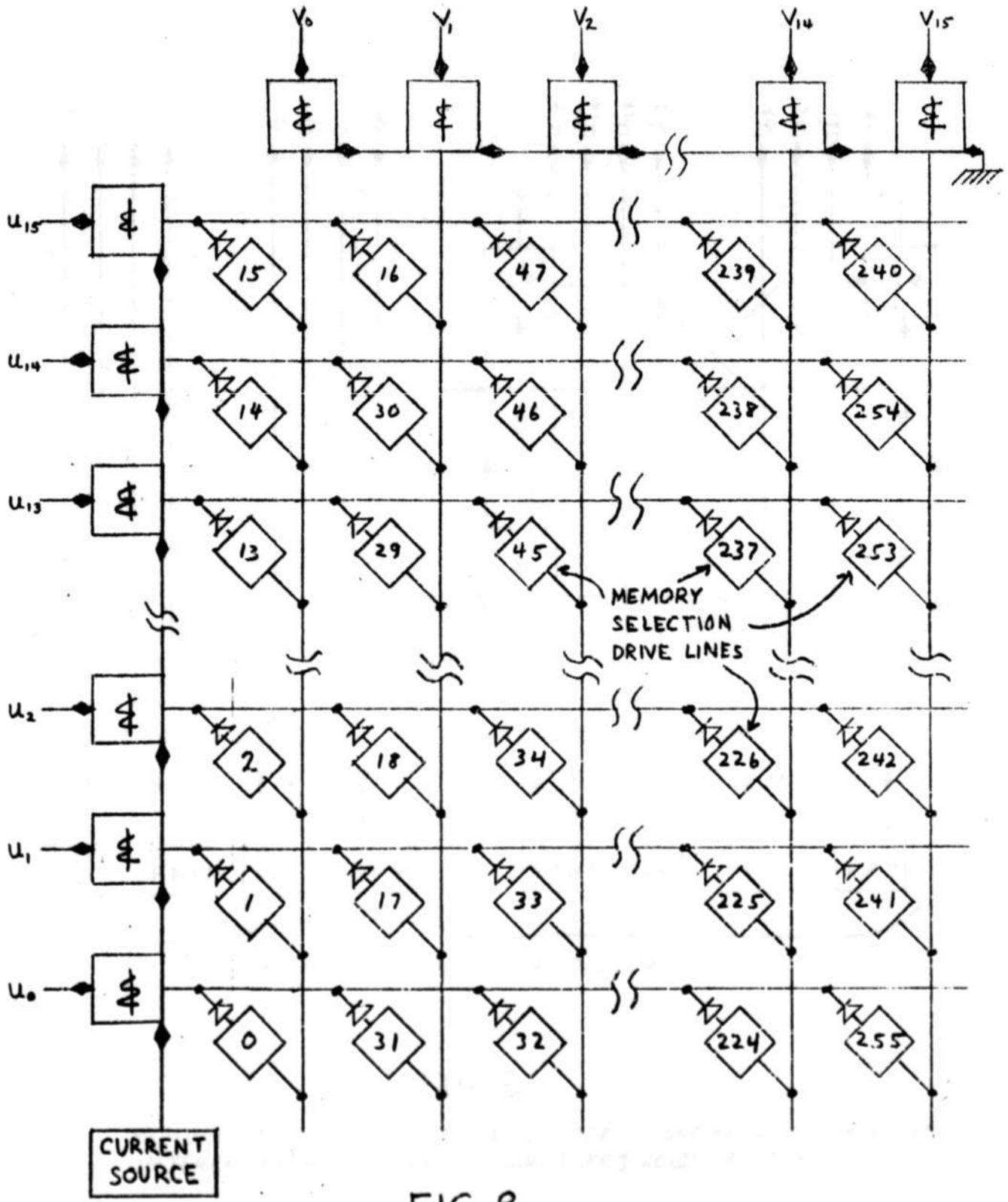


FIG. 8

MEMORY SELECTION SWITCH SHOWING DESIRED ORDER OF SELECTING MEMORY DRIVE LINES

SA-65547

SA 65547

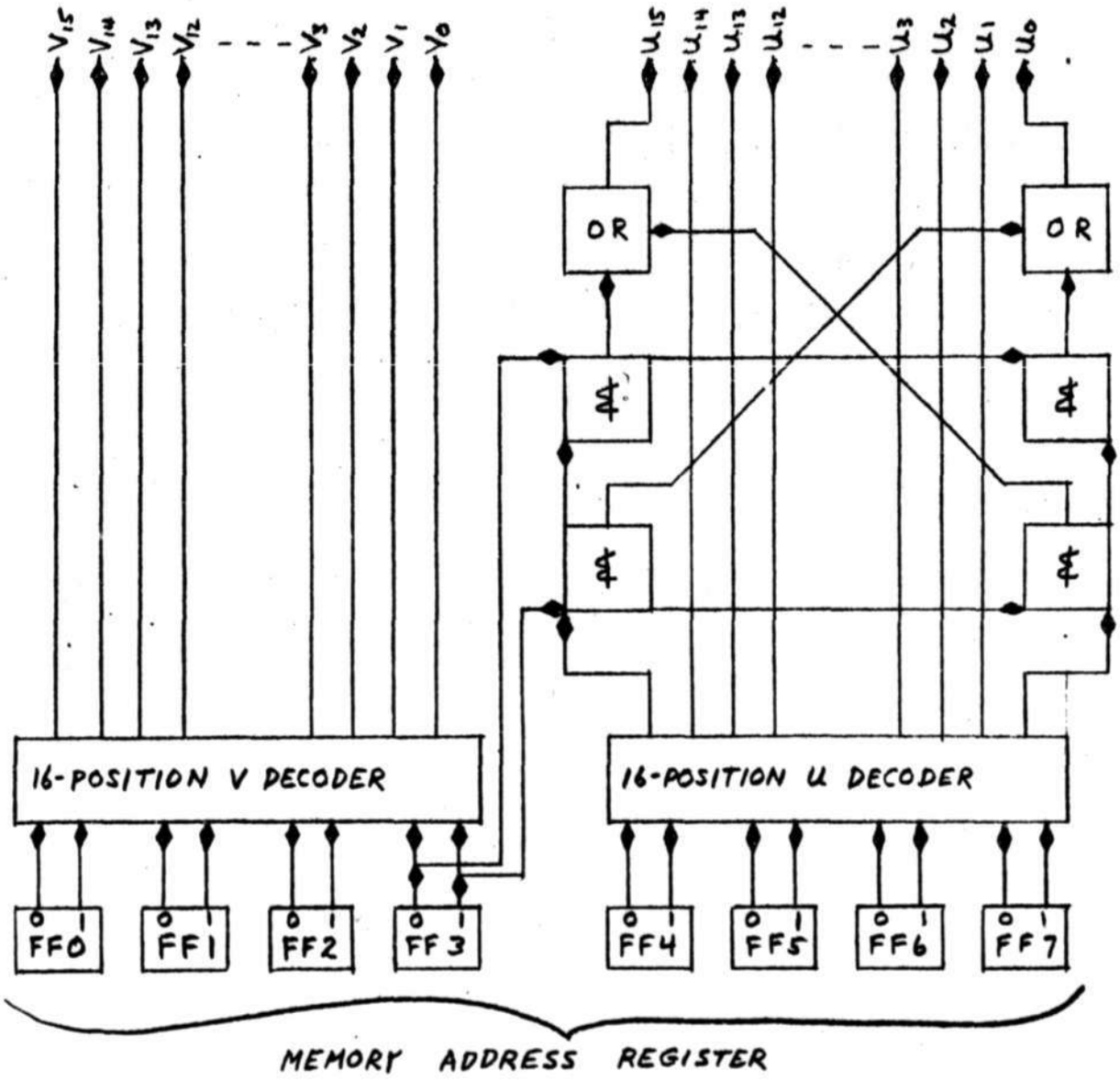


FIG 9

MEMORY ADDRESS REGISTER DECODER SHOWING METHOD OF INTERCHANGING U_0 AND U_{15} WHEN FF3 HOLDS A "ONE"

SA-65548

SA-65548