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SUBJECT: XD-1 EVALUATION, 20 MAY 1955

To: N. H. Taylor

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Abstract: The CD side of the drums has been systems tested and is now part of the XD-1. However, as anticipated by the drum system engineers, the drums performed very poorly during the evaluation tests.
The percentage of usable assigned time was 73% during the time assigned to MIT and 74.5% for the time during which IBM was running reliability programs and utility programs. Most of the low margins found during the last evaluation have been improved. In general, the reliability of the central computer has improved slightly since the last evaluation was made.

I. Physical and Logical State of XD-1

The magnetic tape equipment, drum system, and the magnetic core section of the manual input system have been connected into the XD-1 system since the last evaluation of XD-1 was made. The tapes, core inputs, and the OD section of the drums (the section connected to the in-out equipment) are now being systems tested; i.e., tested as a part of the XD-1 system. The central computer, core memory, card machines, and the CD section of the drums (the section connected to the central computer) now comprise the XD-1 system. The evaluation on May 20 covered the sections of the XD-1 system that were not being systems tested.

With just the CD side of the drums available, only the addressable fields could be tested. The RD fields and the DD field were not working at all and some of the AM-B fields and TD fields contained intermittent troubles. The AM-A drum fields seemed to be OK. However, the drum tests were discontinued because so many fields were failing.

Programs RMM 204, SY 001 and RCM 03 were used to test the central computer. Program SY 001 combines programs RAE 01, RCM 01, and RMM 204; these programs test the arithmetic element, card machines, and memory,

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respectively. SY 001 also tests the computer's ability to mix break cycles with computer cycles. RCM 03 tests the ability of the punch to punch a "worst pattern" on the cards; it also tests the two PER instructions used with the punch.

Program RCC 03, the manual operations test program, could not be run because of a program error. Therefore, the sections of the central computer that were not tested in the previous tests could not be tested during this test.

Programs RMM 204 and SY 001 could not be used to test memory #2 because of some experiments that had been performed on this memory.

Additional cam-operated circuit breakers have been added to the punch to break the circuits to the punch magnets. This reduces the current through any one breaker and has improved the operation of the punch very much.

A set of brushes in the second reading station of the card reader has improved the operation of the card feed mechanism in the reader. Cards containing a very large number of punches can now be read.

It is no longer necessary to turn off the power to the card reader to get that unit out of an in-out pause; however, the card reader cannot be made "not ready" by pushing the card reader "stop" button. Also, the "master reset" button will cause the card reader to feed one card when cards are in the card feed.

The new two-megacycle oscillator has been installed in the instruction control element.

The cables to the printer and the punch have been placed in the troughs provided for them and these units are now oriented correctly.

The power supply control buttons and lights on the maintenance console have been connected, but the "air" and "temperature" alarms are not yet wired in.

Two logical changes have been made in the computer. One change causes the parity-alarm-stop to stop the computer so that the incorrect word remains in the memory buffer register. The other change was made in the overflow circuits so that false overflow indications could not occur during divide instructions.

Except for these additions and changes, XD-1 is still physically and logically the same as described in previous evaluation reports (6M-3443 and 6M-3478).

II. Reliability:

In order to determine the reliability of the XD-1 Central Computer, a study of log book entries has been made and an evaluation test lasting six hours was performed.

1. Log Book Data:

A summary of data taken from the XD-1 log entries for the period of 9-20 May 1955 is shown in Table I. Incidents and failures which occurred are found in Table II.

Reliability and utility programs are listed as a system assignment because in many cases it was not practical to determine the assignment for these reliability programs. Included in the forty-seven hours and twenty-three minutes of time listed under reliability and utility programs, are twenty-five hours during which programs ran with no failures noted during the assigned period. The remaining time includes a history of time spent running reliability programs to isolate failures which could have occurred at some previous time.

TABLE I

XD-1 Log Book Analysis - 9-20 May 1955

System Assignment	Assigned Time	Lost Time	No. of Failures
MIT Assigned Time	13 hrs. 38 min.	3 hrs. 41 min.	20
Marginal Checking	10 hrs. 57 min.	1 hr. 15 min.	1
Simulation & Testing	83 hrs. 32 min.	30 min.	5
Reliability & Utility Programs:	47 hrs. 23 min.	12 hrs. 18 min.	17
Maint. & Improvements	60 hrs. 8 min.	3 hrs. 33 min.	3
	215 hrs. 38 min.	21 hrs. 17 min.	46
Time omitted because it couldn't be categorized or some information was missing.	15 hrs.	Unknown	Several parity alarms

	Percentage of Usable Assigned Time	Mean Good-Time Between Failures
MIT Assigned Time	73%	.5 hrs.
Marginal Checking	88%	9.7 hrs.
Sim. and Testing	99.5%	16.6 hrs.
Rel. & Utility	74.5%	2.06 hrs.
Maint. & Improve.	94%	18.9 hrs.

Percentage of Usable Assigned Time

$$100 \times \frac{215.63 \text{ hrs.} -- 21.28 \text{ hrs.}}{215.63 \text{ hrs.}} = 90.4\%$$

Mean Good-Time Between Failures

$$\frac{194.35 \text{ hrs.}}{46 \text{ failures}} = 4.2 \text{ hrs.}$$

TABLE II

XD-1 Failures for 9-20 May 1955 (Excluding MIT Assigned Time)

No. of Failures	Description of Failures
	Alarms
5	Unexplained error stops
3	Unexplained core memory parity errors
1	Unexplained loss of power
2	Unexplained failures to read-in
	Plug-In Units
7	"W" type diodes
4	Checked and no trouble found
2	Resistors
2	Tubes
2	Bad Solder joints
1	Pulse transformer
	Card Machines
2	Printer (actually, the printer failed in position #29 many times. The cause for this failure was known, but final repair was not made because procurement of replacement parts was slow for this particular item.)
	Miscellaneous
1	Marginal checking system inoperative
1	Shock sensitive "emergency off" relay
1	Intermittent cable short
1	Bad solder joint
1	Relay (bad contacts)
1	Wiring error
1	Accidental emergency off

2. Group 61 (MIT) Operation of XD-1:

Programmers from Group 61 (MIT) used the computer for approximately 13 1/2 hours during the two-week period ending 20 May 1955. A summary of computer operation during this time is included in Table III.

TABLE III

MIT's Assigned Time on XD-1

The following data was obtained during the daily operation of the XD-1 Central Computer by programmers from MIT (Group 61):

Assigned Time -- 13 hrs. 38 min.

Lost Time Attributed to:	No. of Failures:	Time Lost:
Printer	4	24 min.
Parity Alarms (unexplained)	4	13 min.
Interruptions From Drum Frame Test	3	30 min.
Card Punch	2	13 min.
Burroughs' Gate and Delay Unit (temporary arrangement)	2	9 min.
Card Reader	1	20 min.
Plug-in Units		
Maintenance found no fault with plug-in unit	1	52 min.
W type diode failure	1	1 hr.00 min.*
Bad solder joint	1	
Bad solder joint on back panel wiring	1	
	20	3 hrs. 41 min.

Percentage of Usable Assigned Time

$$100 \times \frac{13.63 \text{ hrs.} - 3.69 \text{ hrs.}}{13.63 \text{ hrs.}} = 73\%$$

Mean Good-Time Between Failures

$$\frac{9.94 \text{ hrs.}}{20 \text{ failures}} = .50 \text{ hrs.}$$

* The bad solder joints and the W type diode were found as a result of failures during read-in operations from card reader. It was not possible to assign lost time to each failure.

3. Evaluation test - 20 May 1955:

Only 23% of the time used to evaluate the central computer during the evaluation test on 20 May 1955 was "error free." Because program RCC 03 was in error, cards for program SY 001 were missing from the deck, and the printer continued to fail in position #29, it is not possible to calculate the percentage of usable assigned time and the mean good-time between failures. Core memory II was being subjected to special adjustments and tests; therefore, program SY 001 always stopped on a parity alarm when this memory was used.

In lieu of the usual measure of reliability, a list of programs and other pertinent information are presented in Table IV.

TABLE IV

Computer Evaluation Test, 20 May 1955

Program: RCM 03
Total time (useful time and lost time) = 26 min.
Lost time: 4 min.
Failures: PER 73 (failed twice)
Program: RCC 03
Total time: (useful time and lost time) = 1 hr. 34 min.
Lost time: Because of an error in the program, the program was not run successfully.
Program: SY 001
Total time (useful time and lost time) = 2 hrs. 40 min.
Lost time: For one hour and forty-two minutes program SY 001 was run, with some of the program cards missing. During this time, the following incidents were noted:

1. Cards punched during program were in error.
2. A bad neon was found in bit L6 of the IO reg.
3. Position #29 on printer failed to print correctly.
4. The card reader failed to read-in.
5. The master reset failed to make the card reader "ready".
6. Two memory parities occurred.

After the missing cards were returned to the SY 001 deck, the program ran successfully for fifty-eight minutes -- the only error was the failure of position #29 in the printer.

Program: RMM 204
Total time (useful time) = 15 min.
Lost time: None

4. Reliability Analysis

A comparision of reliability figures for the three evaluation tests performed on the XD-1 is as follows:

Percentage of Usable Assigned Time

1 March 1955 - 73.5%
18 March 1955 - 91.5%
20 May 1955 - 90.4%

Mean Good Time Between Failures

1 March 1955 - 4.72 hrs.
18 March 1955 - 3.8 hrs.
20 May 1955 - 4.2 hrs.

The decrease in parity alarms and component failures (1% Stemag resistors) were instrumental in causing the mean good-time between failures to increase. It appears that core memory's operation is satisfactory. Actually, records of operation do not give a true indication of reliability because core memory II was being subjected to special tests, measurements, and modifications. During this time, however, all programs except RMM 204 could be run using core memory II. From a records viewpoint, the four parities encountered during MIT's assigned time (see Table III) are the most significant indications of memory weakness noted during computer operation. The evaluation test on 20 May 1955 also substantiated the fact that parity errors occurred frequently. A special effort is now being made to eliminate any weakness found in the core memories.

Stemag 1% resistors are being replaced in applications where they have shown high failure rates.

Almost 45% of the failures recorded occurred during the time MIT was using the computer. During this time a special effort was made to maintain complete records. Also, programs run during this time exercised the computer quite extensively -- especially the card machines.

There seemed to be no excessive failures attributable to any one particular fault; although card machines and core memory problems caused much lost time during MIT's assigned time. Interference from drum testing activities is also causing lost time.

II. Margins and Margin History

For the period of 9-20 May 1955, weekly margins were taken on the central computer using the manual marginal checking system; programs and associated marginal checking equipment groups were as follows:

Program Used	Equipment Group
RCC 03	MC-3 (Program and Control Elements)
RAE 01	MC-2 (Arithmetic Element)
RMM 204	MC-1 (Core Memories I & II)

A review of margins cited in the 18 March 1955 evaluation (see 6M-3478) revealed that some of the margins which failed to meet the arbitrarily ± 20 percent variation of supply voltage have been improved. The following exceptions were noted:

Equipment Group	Voltage	Margin	Logic	Remarks
2	-300	A	1	The $_{C}$FF's in the Real Time Clock Freq. Div. have exhibited an 8 volt drop in positive margin over the past two months. These margins are now +17 and -53 volts.
2	+90	C	1-3	The GT's in the L and R adder and the $_{A}$GT's in the L and R Acc. (odd bits) have decreased from +25 and -20 volts to +25 and -13.5 volts in two months. This rapid deterioration of margins should be explained.
2	+90	C	4-6	Same as +90 C 1-3 for the even bits of the Adder and Acc.
3	+90	C	1-3 & 4-6	The $_{A}$GT's in the parity circuits are responsible for the low margins on these lines. These margins have decreased from +25 and -18 volts to +25 and -12 volts in two months. This rapid deterioration and low margin should be explained.
1	-150	C	1	The margins on the sense amplifiers for core memory I have changed from +40 and -20 volts to +34 and -19 volts in two months. These margins will be improved with the addition of proposed core memory modifications.
1	-150	F	1	The margins on the sense amplifiers for core memory II have changed from +40 and -27 volts to +21 and -23 volts in two months.

A history of margins is being punched on IBM cards and a margin check data report is prepared from this data. This history now covers a period of about three months, so it is possible to note the variations in margins that have been recorded for XD-1. Only the most significant variations in margins have been noted in this report. More detailed information regarding margins is included in the margin check data report

published by IBM.

One plug-in unit in the R. Acc was removed because of low margins. Records which describe the repair of this plug-in unit were not available, however, histories of all other repaired plug-in units checked for this evaluation were complete. Limits to which margins deteriorate before they are investigated or repaired have not been established; this is one reason for having only one unit removed. Marginal checking has been useful in detecting wiring errors which caused circuits to operate at a point which was less than optimum.

An effort was made by both IBM and MIT personnel to determine how many failures were being found by means other than marginal checking that should have been detected by marginal checking. This study was very time consuming and sometimes resulted in confusion if certain information was missing. The general opinion was, however, that most of the failures were of the type not susceptable to marginal checking; i.e., open transformers, open diodes, broken tube bases, etc.

Present improvements and changes in processing data from XD-1 logs increase the feasibility of determining the effectiveness of marginal checking by finding out if units which are being marginal checked have failed before margins have shown them to be questionable. Because it is easier to obtain information with the records soon to be made available, these studies should be continued. Also, the results of component failure analysis should be made available to people responsible for this study at the earliest possible date.

IV. Shock Tests

No shock tests were performed during this evaluation. However, it has been noticed that transients caused when power is switched on or off at the drum frames or tape frame will cause errors in the operation of the core memory.

V. Conclusions

We were warned by the IBM engineers that the drums were not ready to be tested, and they were right. The drums performed so poorly that the evaluation tests were discontinued. Although systems tests on the CD side of the drums are officially finished, some more work should be done before the drums are considered to be ready for use.

The number of unexplained memory parities has been reduced slightly since the last evaluation. The number of card machine errors has increased; this increase is probably due to the increased use of the card machines by the MIT programmers, and to changes made in the in-out control circuits to accommodate the warning lights. The operation of the reader and the punch has actually improved since the last evaluation, but the printer appears to be less reliable than before. The central computer reliability continues to be good.

Most of the margins on the central computer and memory are good. The new 2 mc oscillator has good margins. There are three exceptions -- gates connected in long chains, cFF's, and memory sense amplifiers. Long chains of gate tubes, which are checked by applying margins to every other circuit in the chain, are expected to have relatively low margins; but it is hoped that these margins will be improved. Modifications to the sense amplifiers have already been proposed. There are very few cFF's in the central computer, so accurate conclusions concerning them cannot be made.

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