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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: GROUP 63 APPROVAL COMMITTEE MEETING, MAY 31, 1955

To: Group 63 Staff

From: David R. Brown

Date: June 1, 1955

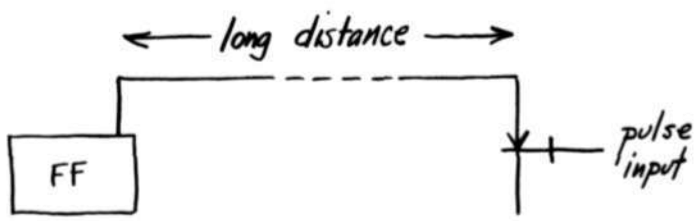
Present: D. R. Brown, W. A. Clark, E. U. Cohler, N. L. Daggett, J. W. Forgie, T. H. Meisling, and K. H. Olsen

Agenda:
1. Emitter-Input Gates
2. Symbols
3. Next Meeting

1. Emitter-Input Gates

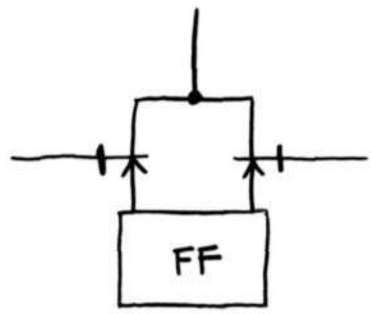
Although some saving in transistors might result from the use of emitter-input gates, they will not be used. Base-input gates will be used. Use of emitter-input gates would lead to the following difficulties:

a. In some cases, pulses would have to be transmitted over long distances.



b. Sneak paths could short from one flip-flop output to the other. In the case shown here, both gates can be on at the same time.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

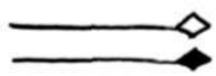


c. More transistors may be required in series.
d. A heavier load current is drawn from the flip-flop.

2. Symbols

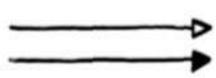
Wes Clark proposed a set of symbols in which open and solid arrows are used to tell whether the one state is to be associated with ground potential or a negative voltage.

levels:



one when at ground
one when negative

pulses:

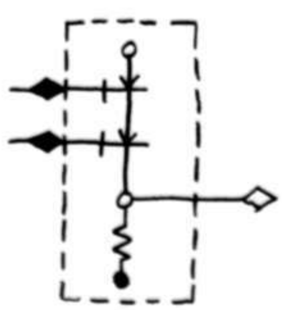


one when at ground
one when negative

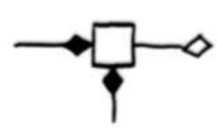
inverter:

or

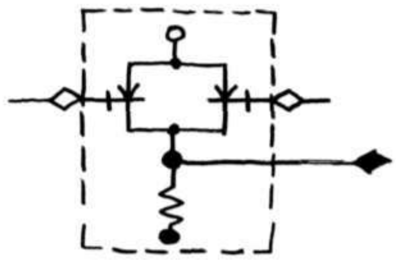
series gate:



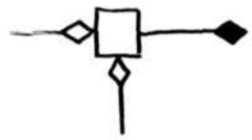
or



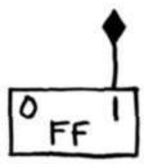
parallel gate:



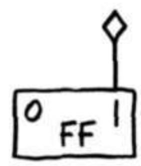
or



flip-flop output:



negative when FF holds 1



at ground when FF holds 1

More consideration will be given these symbols before a set of symbols is approved.

3. <u>Next</u> <u>Meeting</u>

The next meeting will be held on Friday, June 3, to approve the circuits for the multiplier logical plug-in unit and the flip-flop circuit.

Signed: David R. Brown
David R. Brown

DRB/dg

cc: R. R. Everett