

Memorandum M-2842

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SUBJECT: XD-I DIGIT-PLANE DRIVER

To: N. Taylor

From: D. Shansky

Date: 28 May 1954

Abstract: A self-balancing bridge is utilized in conjunction with an "and" and an "or" gate input to satisfy the wave form and gating specifications on the driver for a magnetic core memory digit plane winding.

The digit plane driver is a circuit which combines the logical function of both an "and" and an "or" gate with a regulated pulse current source. For purposes of an explanation of circuit operation it is most convenient to simplify the discussion by describing the operation of the 2 logical blocks independently of one another.

Regulated Pulse Current Source.

This portion of the circuit consists of 5 cathodes in a feedback loop. Two of these cathodes are in a difference amplifier ( $V_{2II}$ ,  $V_{3I}$ ), which serves to compare a signal voltage produced by current  $I_{II}$ , flow through a sampling resistor, to a constant voltage level established by a potentiometer connected across a power supply. A third cathode ( $V_{3II}$ ) serves to amplify and invert the output voltage of the difference amplifier and drive the grids of the final tube ( $V_{4I,II}$ ), which is a 5998. The cathodes of the difference amplifier are normally held up to  $\pm 10$  volts by a cathode follower ( $V_{2I}$ ), so that these tubes are normally cut off. The inverter-amplifier tube ( $V_{3II}$ ) is normally conducting, while the driver tube ( $V_{4I,II}$ ) is normally cut off by the presence of a large negative bias. During the pulse, the cathodes of the difference amplifier ( $V_{2II}$ ,  $V_{3I}$ ) are allowed to fall by applying a negative gate to the grid of the cathode follower ( $V_{2I}$ ) whose cathode is connected to the cathodes of the difference amplifier. Therefore, the plate of the difference amplifier will fall and the change in voltage will appear at the grid of the normally conducting inverter. The plate of the inverter-amplifier ( $V_{3II}$ ) will rise at a rate determined by the plate load resistor and stray, input and output capacities. This change in voltage will be coupled over to the grids of the normally off 5998 turning them on. The voltage developed across the sampling resistor ( $R_{29,30}$ ) by current flowing through the 5998 and the load is fed back to the difference amplifier where it is compared to a reference voltage applied to the other grid of the difference amplifier. During the pulse then, this regulated pulse current source becomes a self-balancing bridge. The back voltage produced

by the load is fed back to the difference amplifier (via  $C_8$ ) as a common mode signal to insure an adequate current source regardless of load variation.

This particular geometry has resulted in a circuit which has extremely broad tolerances with respect to tubes, component values, and supply voltages, as the accompanying curves indicate, since the circuit inherently adjusts itself to compensate for these variations.

Figure #4, 5 and 6 portray the operating margins of the cathodes in the feed-back loop. The bias on the 5998 output tube was chosen as the marginal checking voltage in each case since the internal loop gain may most conveniently be changed by varying this voltage. A curve on  $V_{2II}$  (the cathode follower portion of the difference amplifier) is not included because it was found that the plate supply of this tube could be made negative with respect to the cathode without causing failure. A diode is all that is apparently necessary here. (By way of explanation of this apparently superfluous cathode, I might point out that the specification on output current change was originally  $\pm 2\%$ . This cathode was included to minimize the change in output current due to variations in contact potential of the difference amplifier. However, in view of the fact that unit failure had to be related to system failure, and in view of the experience gained in M.T.C., failure was defined as a 15% change in current.) In the case of tube  $V_3$  failure was defined as change in output pulse rise time of  $\pm 0.2 \mu\text{sec}$ . This change in timing is compatible with system requirements. Failure was defined in similar manner for all the other cathodes in the circuit with the exception of  $V_1$ , where the failure was evidenced by a 15% change in output current.

#### "And", "Or" Gate Circuitry.

Since it was necessary that the grid of  $V_2$  be allowed to fall more than forty volts because of the common mode signal on the difference amplifier ( $V_2, V_3$ ) produced by the back voltage developed in the load, it was necessary to provide some amplification of the input signal (Flip-Flop output). A 7AK7 was used to provide the necessary amplification and perform the "and" gating function. The output of the "and" gate is fed to a diode negative "or" gate. The other input to the negative "or" gate is connected to the "Post-Write-Disturb" gate generator, which provides a negative going gate of the proper amplitude ( $\pm 10$  to  $-40$ ).

The margins of operation of the 2 cathodes in this portion of the circuit are shown in figs 2 and 3. In the case of Tube  $V_2$  failure was defined as a change in timing as previously mentioned, while failure of the 7AK7 manifested itself as a change in output current.

#### Conclusion

As a result of the experimental work which was done in garnering the information upon which the preceding report was based, it became apparent that a redesign of the unit could eliminate some cathodes and

ease the input driving requirements. The Digit Plane Driver has therefore been redesigned so as to eliminate two cathodes and operate from standard voltage levels. This work was not completed in time to meet the XD-1 production schedules. A report on the improved version of this circuit is being prepared and will be forthcoming shortly.

SIGNED David Shansky  
D. Shansky

APPROVED R. L. Best  
R. L. Best

DS:jb

Attached

Fig 1 B-59149

Fig 2 - SA48525-G

Fig 3 - SA48523-G

Fig 4 - SA48527-G

Fig 5 - SA48526-G

Fig 6 - SA48524-G

B-59149

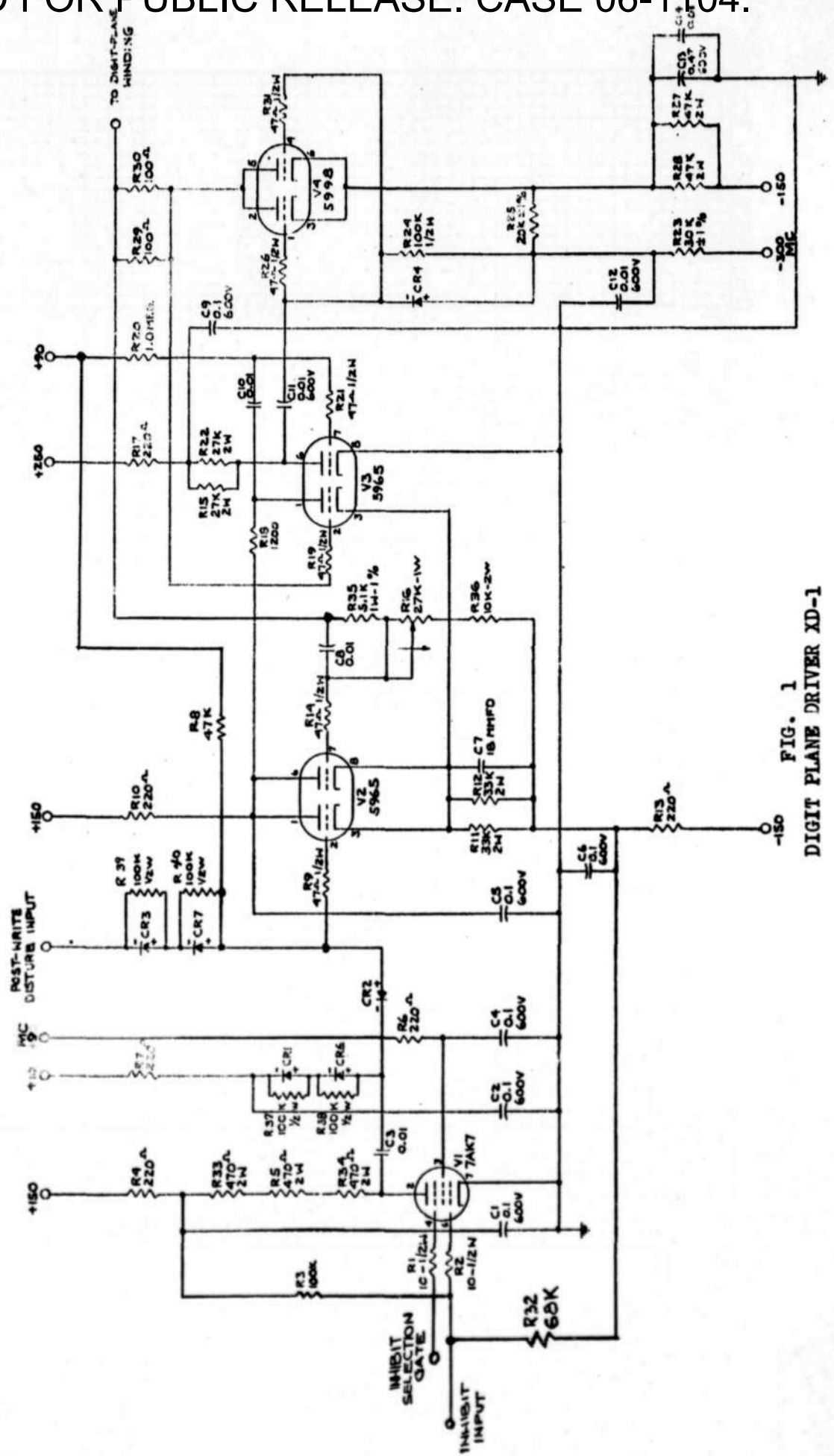


FIG. 1  
DIGIT PLANE DRIVER XD-1

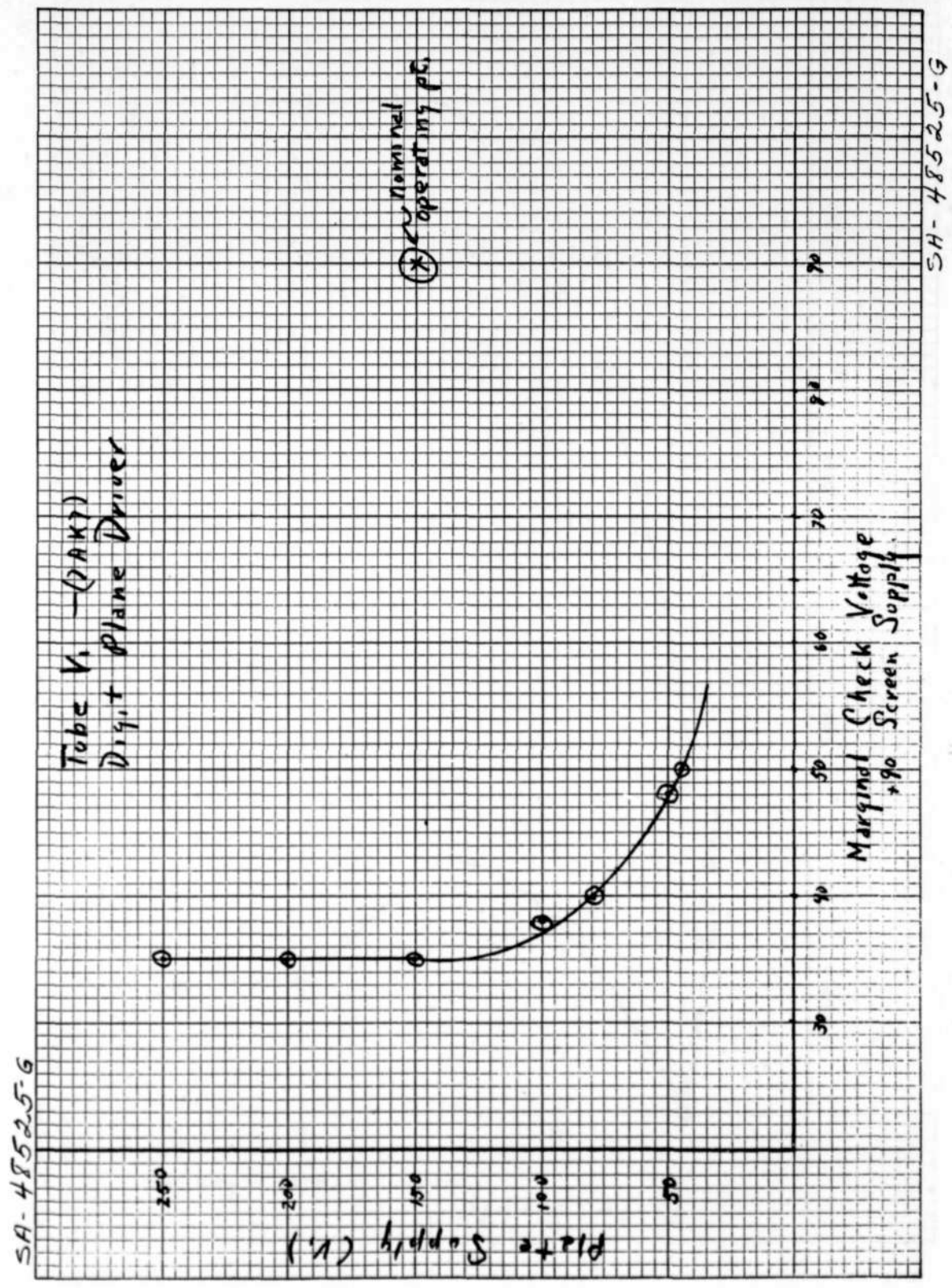


FIG. 2

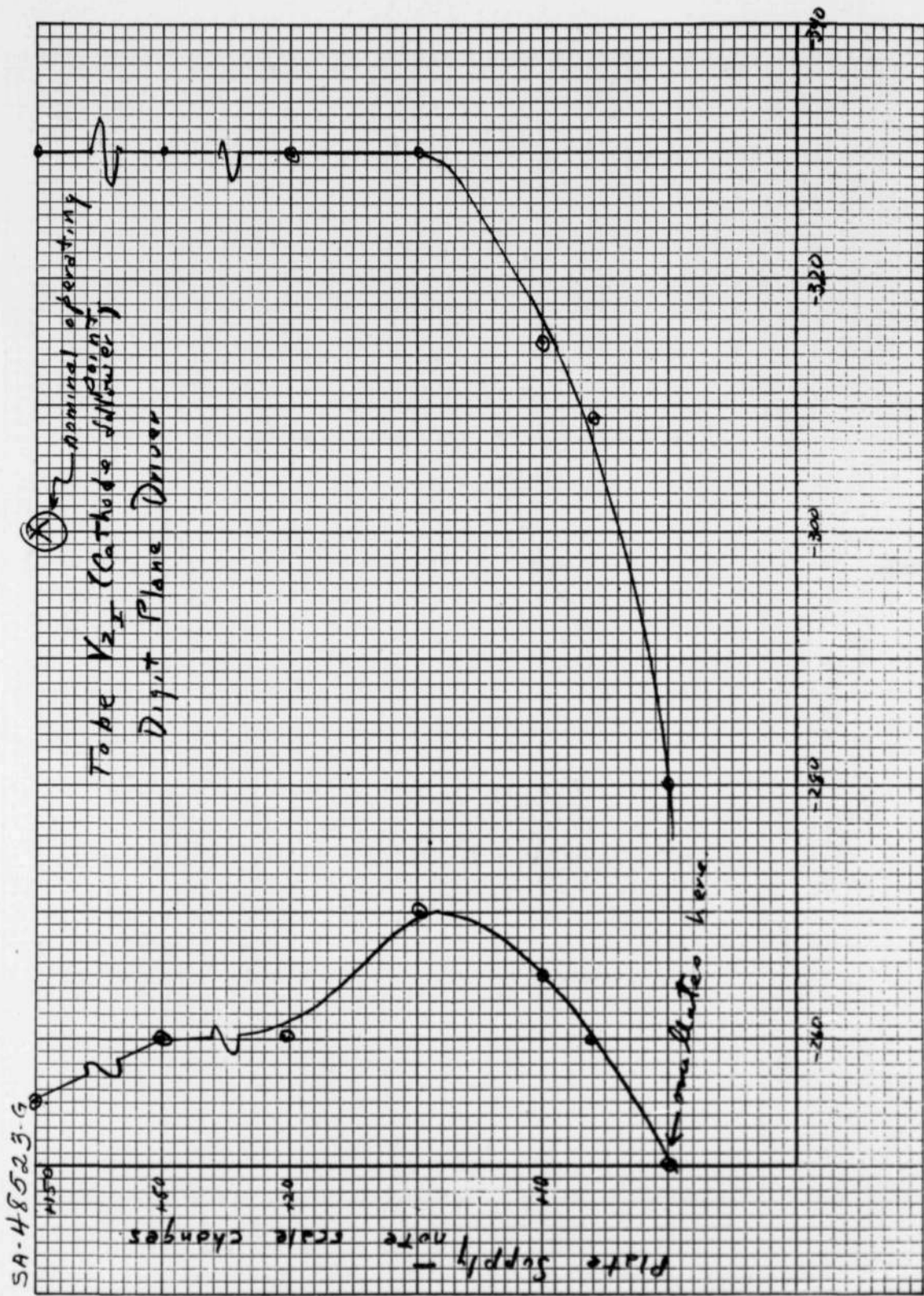
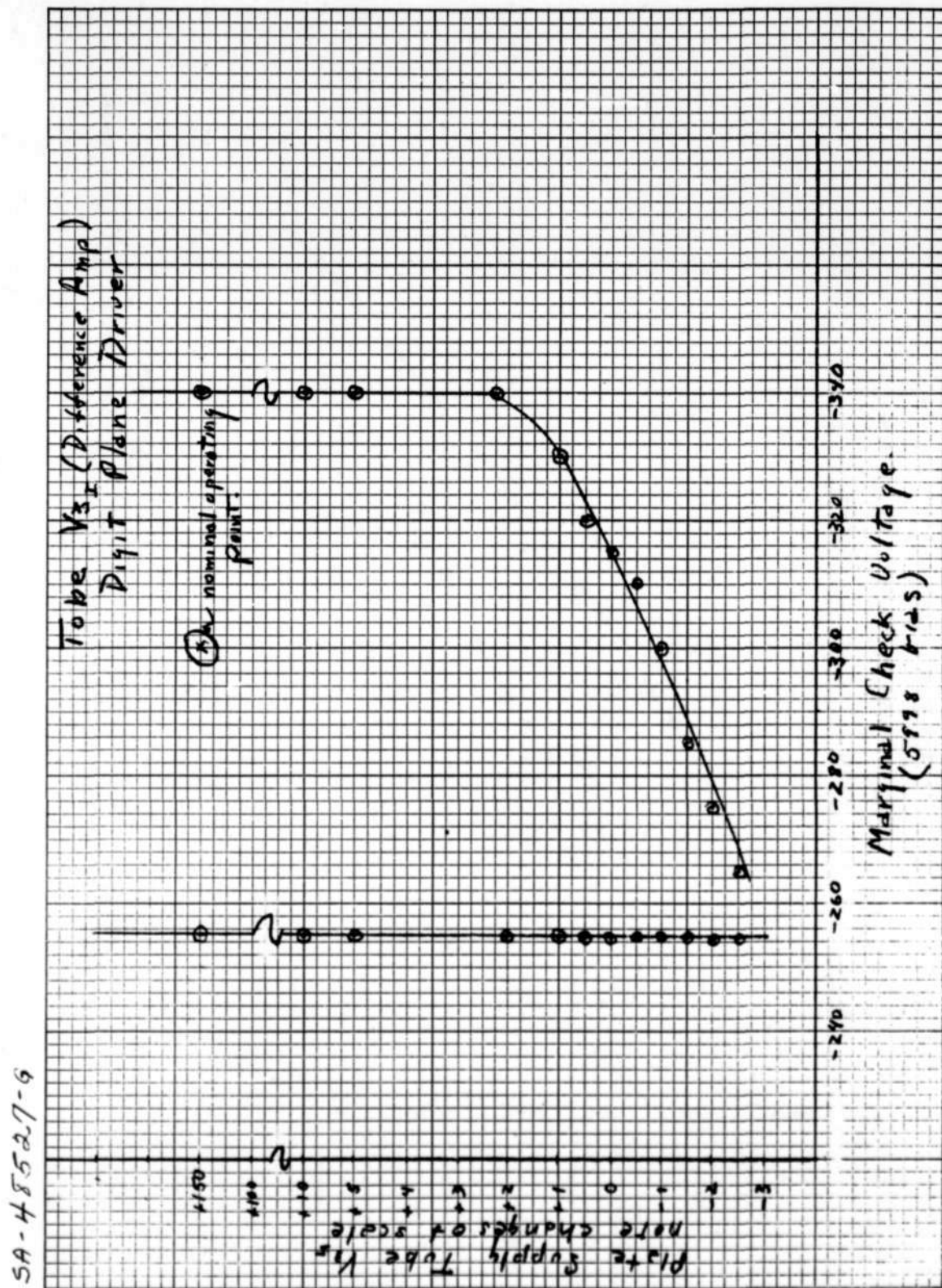


FIG. 3



SA-48527-G

FIG. 4

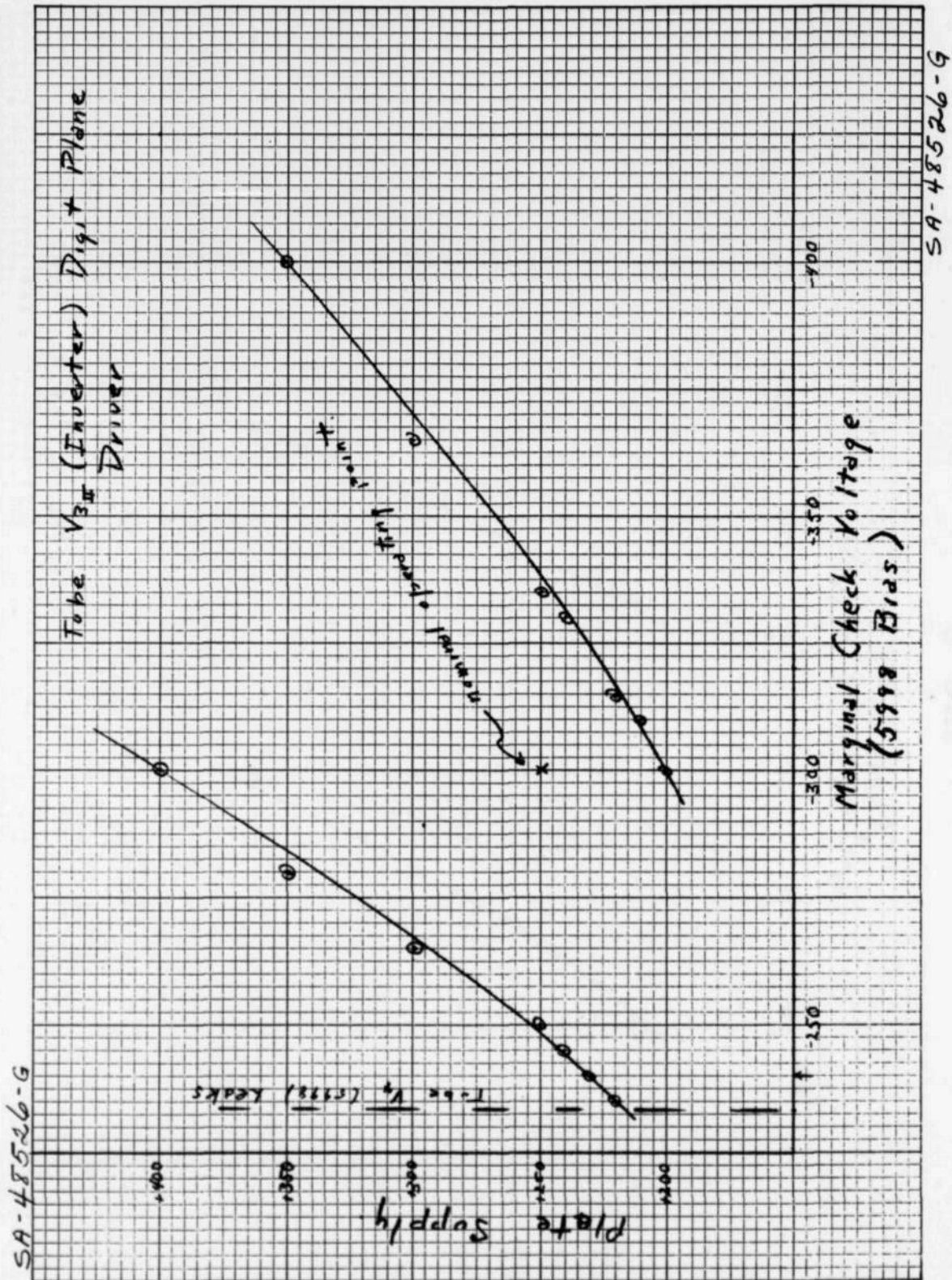


FIG. 5

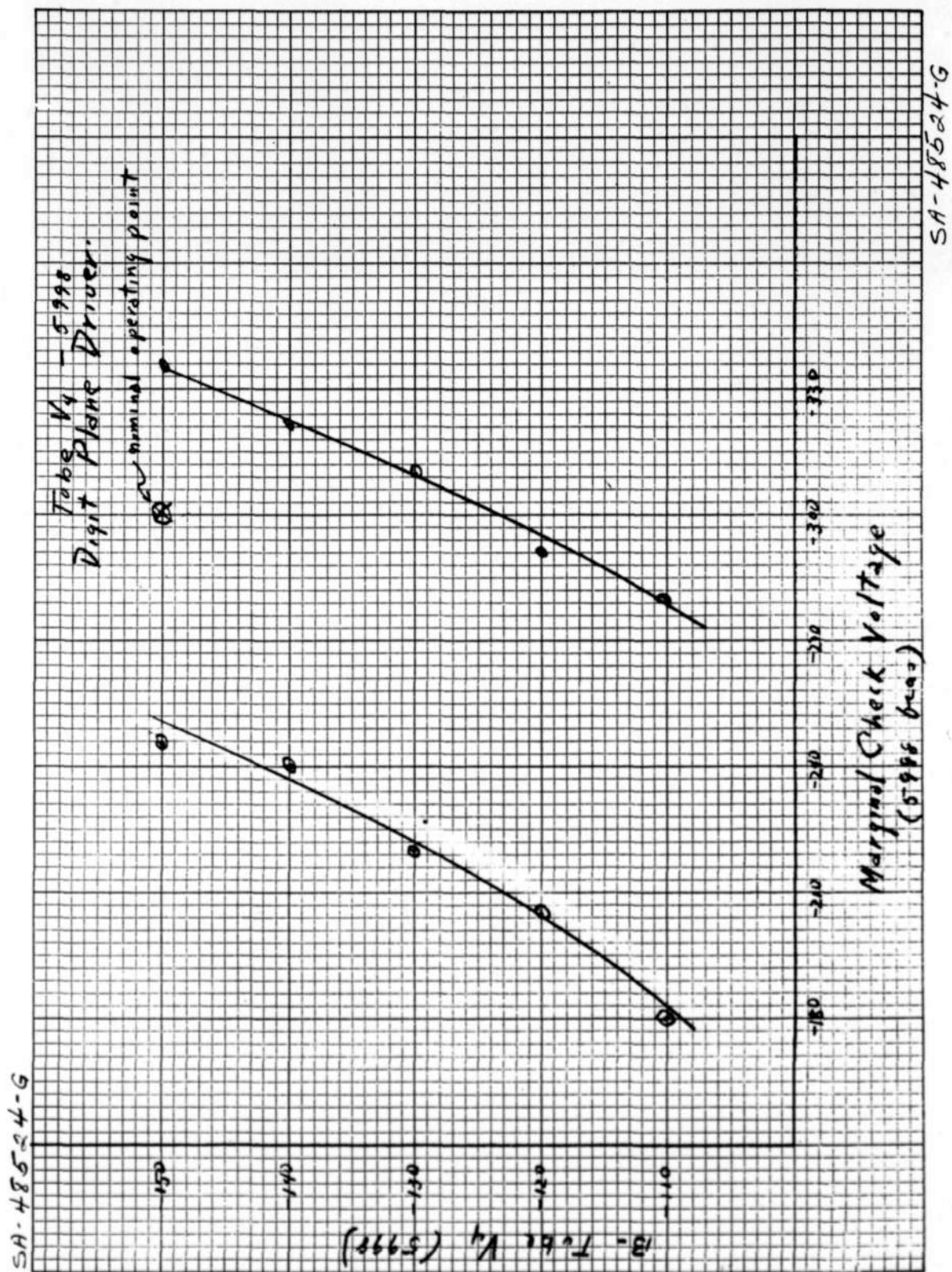


FIG. 6