Earle K. Gates
January 5, 1954

MASTER'S THESIS PROPOSAL

TITLE: Transformer Drive for a Coincident-Current Magnetic Memory

STATEMENT OF THE PROBLEM

The purpose of this thesis is to design a current step-up pulse transformer to drive a magnetic core memory and then to evaluate this method as compared to the direct vacuum-tube drive method used in WWI.

HISTORY OF THE PROBLEM

In 1949 J. W. Forrester[1] proposed a method for the storage of binary information in a three-dimensional magnetic core memory. This method utilized the retentivity (residual magnetism) of magnetic materials and the ability of the magnetic core to discriminate between two different applied fields. A core with a square hysteresis loop is most ideal for this application.

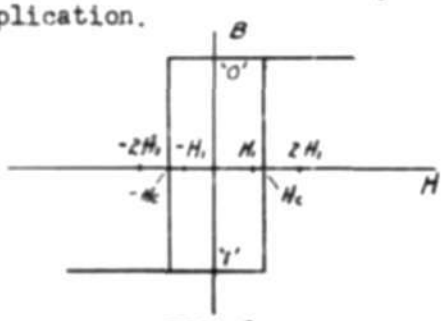

FIG. 1

Figure 1 represents the hysteresis loop of the ideal core material. Assume that the core is in the upper magnetic state so that a "zero" is stored. If we apply a positive field (read pulse) there will be no change in flux and no voltage induced ($e=N\frac{d\phi}{dt}$). However, if the core is in the lower state so that a "one" is stored the application of a positive field greater than H_c will switch the core from the lower to the upper state resulting in a large change in flux and a large induced voltage. If we sample this induced voltage we can determine whether a zero or one was stored in the core. We may write a "one" back into the core by applying a negative field greater than H_c.

When more than one core is involved we must be able to select a particular core to read in or write out information. This may be done by wiring the cores in a grid or matrix as in Fig. 2

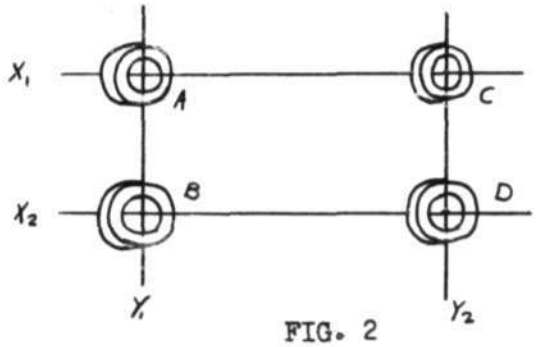

FIG. 2

If a current sufficent to produce a field of magnitude H_1 is sent down any one line (x or y) there will be no change in flux in any core no matter which state the core is in. If a current is applied to both an x and y (say x_2 and y_1) line in such a direction as to produce aiding magnetic fields, then core B will be selected for either reading or writing information, whichever is desired. This is known as coincident current selection. Any size matrix may be driven by this two-dimensional scheme.

If we now stack several matrices or planes together with the x and y lines in series we have a three-dimensional problem of selection. Not only must we select a core at the intersection of an x-y line in each plane, but we must select in which plane or planes we want a corresponding core to be selected. In this way we can represent in binary form a number or word with length determined by the number of planes in the stack or array.

Plane-selection is accomplished by threading a separate wire called a Z winding thru every core in each plane so that when current flows in this wire it will produce a magnetic field in the same relative direction in each core.

By setting up a magnetic field H_1 opposing the field $2H_1$ produced by the x-y lines this particular core will be unselected since only a net magnetic field of H_1 is applied. Therefore any plane can be selected by not sending current thru the Z-winding of that plane.

The pulse required for switching the cores has been determined in the MTC. It should have 0.5 μsec. rise and fall times with a flat top 1.5 μsec. long producing a mmf. of about 0.5 amp. turns. In the desire to keep the construction of the memory simple the memory is made with single turn windings so that 0.5 ampere pulses are required for each x, y and z winding.

The present method uses vacuum tubes to supply this current. Two tubes in parallel are needed to keep within the ratings of acceptable tubes. Also, because we must apply positive and negative fields each x and y line requires two wires since the vacuum tube conducts in only one direction.

PROPOSED SCHEME

In an effort to reduce the tube count and size of tubes necessary for driving the memory it was decided to use pulse transformers with a current step-up from tube to memory. By making this a push-pull transformer it is possible to obtain positive and negative pulses thus requiring only one wire for each x and y line of the memory.

One of the main problems of pulse transformer design is the negative overshoot following the desired pulse. This results because the time integral of the induced voltage must go to zero when the flux has returned to its starting point on the B-H loop. Due to the nature of the logic of the magnetic memory a "read" pulse (positive) is always followed by a "write" pulse (negative). Since the transformer is connected push-pull the overshoot is used as a part of the "write" pulse. After a read-write cycle the transformer does not overshoot because the time interval of the voltage pulse is then zero since the read-write pulses are symmetrical.

The voltage output of a core being switched is very sensitive to the amplitude of the switching current[2] which means that the current regulation of the transformer must be within 5%. It has been determined by H. Rising[3] that a core being switched looks like a variable resistor. The variation in the load then will depend upon the number of cores being switched, (0 to 17) in the MTC).

The solution to the problem is to make the transformer look like a current source to the memory array. A large resistor in series with the load which would have to dissipate a large amount of energy cannot be used because of space considerations. Even though the vacuum tube driving source is a high impedance circuit the transformer reduces this impedance by the turns ratio squared so that we must sacrifice impedance level for current gain.

The design of the transformer must take into consideration this variable and nonlinear load.

PROCEDURE

A. Design and construction of the transformer

The first transformers will have to drive a dummy-load until the memory for MTC is constructed. Among the factors to be determined are: turns ratio, number of turns, core material, damping resistors, load resistor, equivalent circuit for push-pull transformer, and a method of representing the nonlinear and variable load of the array.

B. Transformer driving the memory in an actual computer.

The memory will consist of 17-64 x 64 planes. This will require 128 transformers whose output current must be uniform within 5%. Thus selection of cores before manufacture and control of manufacture will be an important factor in the overall operation of the memory.

C. Evaluation of the system

This system will be compared with the present method of vacuum tube drive and with several other methods if information is available at the time.

Equipment Needs

All necessary equipment will be available at the MIT Digital Computer Laboratory. Standard pulse equipment will be used and laboratory facilities will be available for construction of any special units.

Estimated division of time:

1.	Preparation of proposal	50	hours
2.	Further study of the literature	25	hours
3.	Experimental work and analysis	150	hours
4.	Correlation of results and formulation of conclusions	100	hours
5.	Preparation of thesis report	75	hours
6.	TOTAL	400	hours

SIGNED: Earle K. Gates
Earle K. Gates

DATE: January 5, 1954

EKG/rb

SUPERVISION AGREEMENT

The problem described herein seems adequate for a Master's thesis. The undersigned agrees to supervise the research and evaluate the thesis.

SIGNED: William K. Linvill
Prof. W. K. Linvill
MIT Staff Member

BIBLIOGRAPHY

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2. Hughes, A. D., "Testing of Individual Cores in MTC Planes", MIT Digital Computer Laboratory Report - M-2219.

3. Rising, H. K., "Magnetic-Core Pulse Amplifiers for Digital Computer Applications", MIT Digital Computer Laboratory Report, #2392.

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