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SUBJECT: PROPOSED CHANGES IN FSQ-7 MEMORY

To: N. H. Taylor

From: D. Shansky

Date: July 13, 1954

Abstract: A significant reduction of the cathode count coupled with an increase in operating speed of the FSQ-7 Memory banks can be achieved by a redesign of some of the sections of Memory. In order of increasing difficulty these are: the Digit Plane Drivers, the Sense Amplifiers, and the address selection system. Approximately 6 man-months of engineering time would be required to effect these changes.

Introduction

In view of the changes being made in the prototype machine for scheduled inclusion in the first duplex central, it seems appropriate at this time to outline some changes in Internal Memory which would contribute to the overall reliability of the machine through a reduction of the cathode count of the Memory almost by a factor of 2. These changes could be made without sacrificing existing operating margins.

The proposed improvements to Memory can be categorized as those which can be made by replacing existing pluggable units with new ones (namely the Digit Plane Drivers and the Sense Amplifiers) and those affecting the physical appearance and detailed design of the "Shower Stall" (changes in the selection system).

Digit Plane Driver

A new Digit Plane Driver is already in existence and the major portion of the work to be done on this circuit has already been done. The new Digit Plane Driver offers an increase in system reliability by virtue of having two (2) fewer cathodes per Driver as well as having significantly fewer components. Its operating margins will be roughly equivalent to the older driver. Approximately 1 man-month is the estimated time required to package and test the prototype unit.

Sense Amplifier

Although the present sense amplifier is adequate, a new one, which does substantially the same job at a cost of seven (7) fewer cathodes per unit, has been developed and is presently being tested. It is felt that the investment of a little time in this new amplifier would result in its acceptance for inclusion into the duplex central Memory. The estimated time required, inclusive of packaging and prototype testing, is approximately 2 man-months.

Selection System

One of the major difficulties in the present selection system is the result of the extremely large amount of capacity which the Read-Write Gate Generator is required to drive. This capacity has the effect of reducing the source impedance presented to the pulse output transformer by a given selection-plane driver tube. A secondary detrimental effect of this capacity is the increased circuit delay which it causes. (Almost a full microsecond is required to establish current in the memory.) In an attempt to alleviate this condition, a recent study of selection systems was initiated. The number of Gate Generators was increased in order to reduce the capacity which a given Gate Generator is required to drive. At the same time the number of Matrix Output Amplifiers was reduced. Figure I is a block diagram of this system.

Happily, this contemplated system requires far fewer cathodes than the old system (192 compared to 304). The new circuits which would be used as Matrix Output Amplifiers and Read-Write Gate Generators will not be as critical with respect to input levels as were the older circuits, and since the 32-position crystal-diode matrix would no longer be used for address translation, (2 8-position crystal-diode switches are used instead) the Memory Address Register cathode followers, which presently consist of 9 cathodes per F.F. output (216 total), could be redesigned to use at most 3 cathodes per F.F. output (72 total).

Three units in this system require some further development time (the Matrix Output Amplifier, Memory Address Register Cathode Followers, and Read-Write Gate Generators). In addition, the Selection Plane Driver panels would be redesigned, since all that will appear on these panels would be 5998's and pulse transformers, eliminating the need for plug-in Selection Plane Driver Panels. The engineering time required is estimated at approximately 1 man-month per unit in addition to the time required to alter the mechanical design of the existing memory stall and Selection Plane Driver Panels.

Conclusion

A large number of cathodes may be saved (about 300) by replacing the existing Digit Plane Drivers and Sense Amplifiers with new ones. These changes would not necessarily affect the present back-panel layout or module-space assignments.

260 additional cathodes could be saved by redesigning the selection system. An increase in operating speed as a result of increased selection speed as well as reduced circuit delays is also in the offing. These changes would affect back-panel layouts as well as module space assignments. They would not, however, require an increase in the presently available module space, but would in fact require less room.

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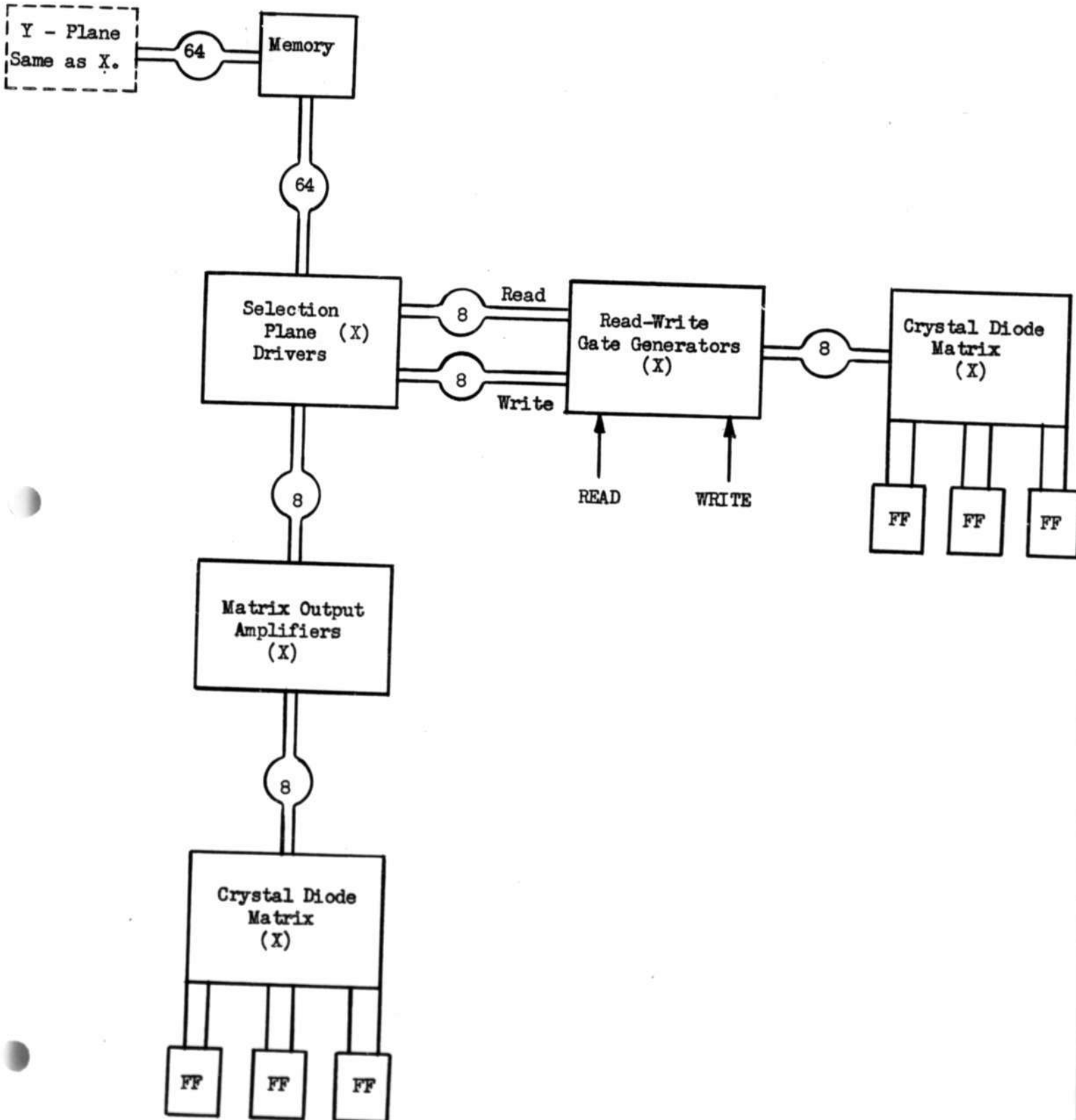
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Magnetic Memory Section

Attached: Figure I.

Figure I

PROPOSED CHANGES IN FSQ-7 MEMORY



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