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SUBJECT: CORE MEMORY USING EXTERNAL BIT SELECTION *

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From: J. Raffel

Date: March 18, 1954

Abstract: A memory system in which the memory function (remanence) and the selection function (nonlinearity) are performed in separate cores may have the following advantages over the present (coincident-current) system:

1) Much broader tolerances on core acceptability

2) Reduced noise out of the memory array

3) Larger signals out of memory

4) Shorter memory cycle time

Some of the costs may be:

1) Two or three times as many cores required

2) More complex construction problems

## 1. Statement of the Problem

Consider the problem of using switch cores to perform the selection function for a magnetic core memory completely external to the memory cores themselves.

## 2. The Functions This Selection System Must Perform

It must be capable of subjecting any memory core in a selected register to either of two cycles:

Read, Write ZERO ($R\text{-}W_0$)

Read, Write ONE ($R\text{-}W_1$)

without exciting any other cores in the array.

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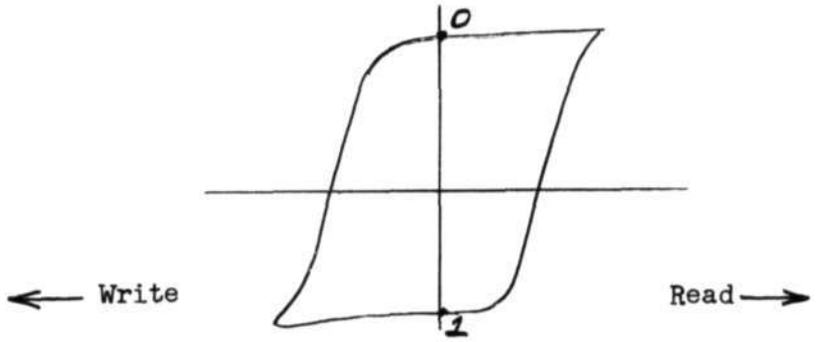
* This note is a section of a thesis to be finished shortly which will deal with the general problem of register selection.

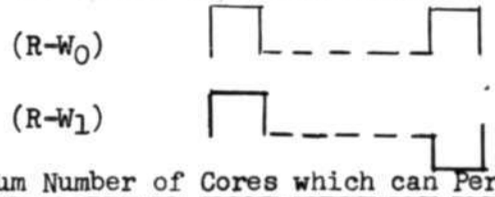
(A ZERO and a ONE are represented in the usual manner as shown on the hysteresis loop below along with Read and Write polarities.)




3. The Necessary and Sufficient Conditions Imposed on the Excitations which the Switch Cores are to Provide to the Memory Cores.

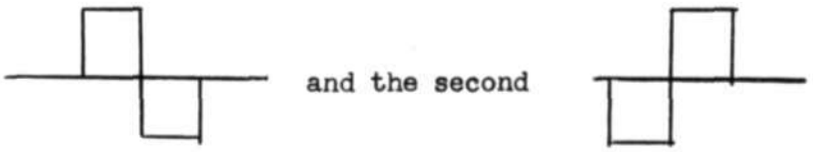
For cycle R-$W_0$ it is only necessary that we have a sequence which has a first pulse plus and a last pulse plus.

For cycle R-$W_1$ we require a first pulse plus and a last pulse minus. These two cycles are shown below.



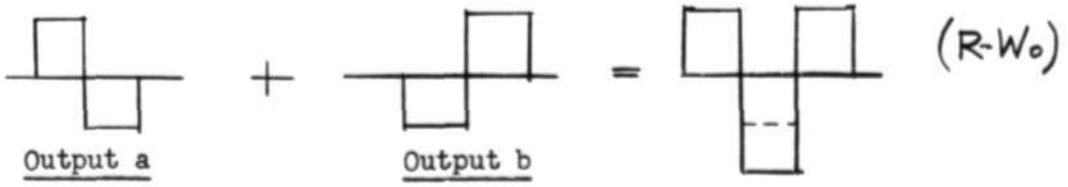

4. The Minimum Number of Cores which can Perform the Switching Function Outlined Above.

We recall that a switch core must be reset to its original flux state before the start of a new cycle; this is a natural for R-$W_1$ cycle. However, the R-$W_0$ cycle cannot come from a single core; it could, though, come from the properly combined outputs of two switch cores, the first of which produced:




Output a Output b.

We then have all we need to obtain the two cycles desired as shown below.




Output a Output b

(If we overlap for minimum time)


Output a

It is also evident from above that the minimum number of switch cores needed is one core per register to supply Output a, (all the cores in the register receive it) and one core per bit to supply Output b, (each core in the register may or may not receive this depending on whether a ONE or a ZERO is being written).

5. Operating Characteristics

By completely separating the switching and memory functions the cores are no longer restricted to the critical requirements on driving current and hysteresis-loop squareness imposed by coincident-current operation. The hysteresis loop required for a coincident-current memory is shown in Fig. 1. The loops required of the switch core and memory cores in the proposed system are shown in Figs. 2 and 3 respectively. The main requirement of the switch core is that it be saturable, of the memory core that it have two distinct remanent-flux states.

In addition to reducing the core uniformity requirements this system makes possible increased signal outputs, shorter cycle times and reduced noise.

6. Physical Realization

The main problem in constructing a memory of this sort is the increased wiring complexity which results from driving each memory core individually rather than from common lines. This requires small coupling loops linking pairs of cores and these may be difficult to fabricate unless done perhaps by machine. One possible configuration is shown in Fig. 4. On one side of a phenolic board are wired switch cores having X, Y, and Z windings as in conventional memory digit plane. Each core is also connected to a corresponding memory core on the other side of the board by a small loop or staple. All the memory cores on a single digit plane have a common sense winding. This takes care of the memory core and the switch core which supplies ouput b described above. All we require now is a single core per register to supply output a. The output of this switch would then go down a line linking all the memory cores in a register successively. From a construction point of view it might be simpler to use one core per bit for output a. The construction of the two switch planes now required per digit would be identical and might lead to simpler winding although more cores are used.

7. Conclusion

This system offers many advantages over the conventional coincident-current method. Its main drawback is construction complexity. Experimental work to obtain a quantitative evaluation in terms of cycle time, core material requirements, etc., would be desirable, since it may find use in some special memory application and if construction difficulties were overcome, as central memory unit for a computer.

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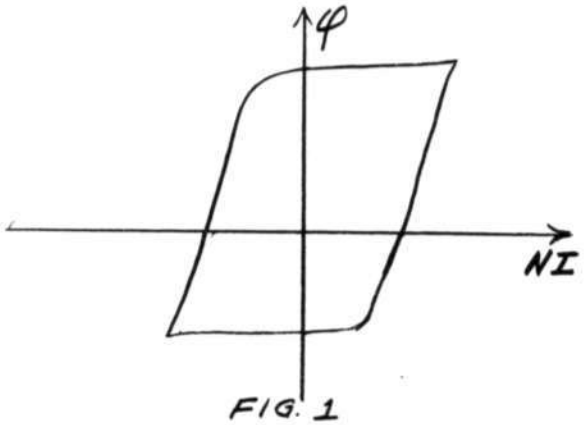



FIG. 1

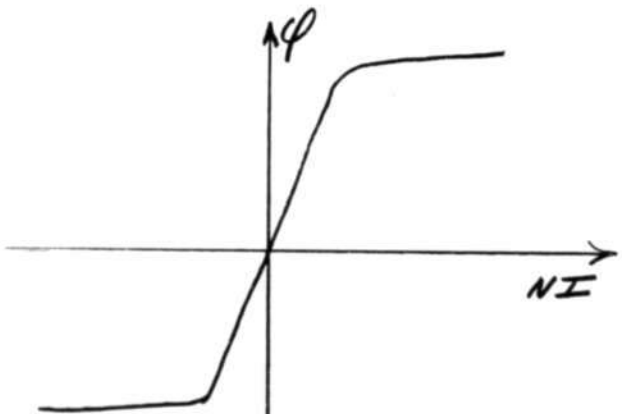



FIG. 2

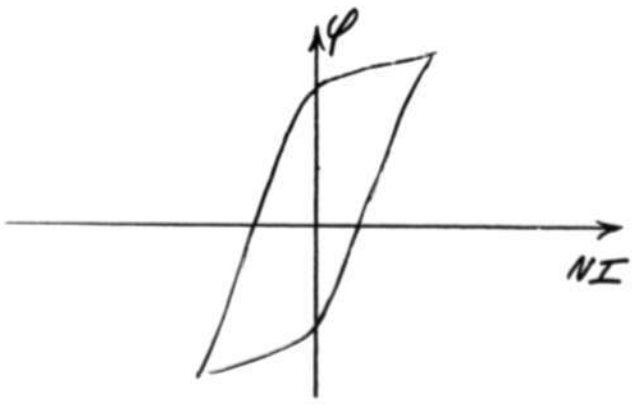
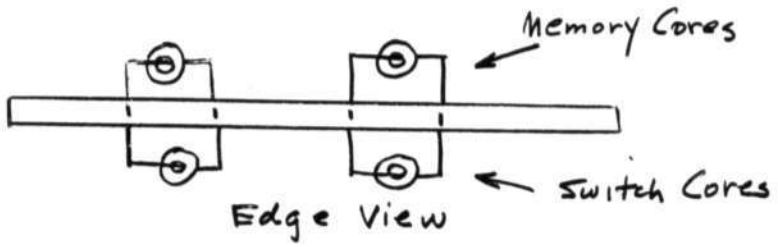
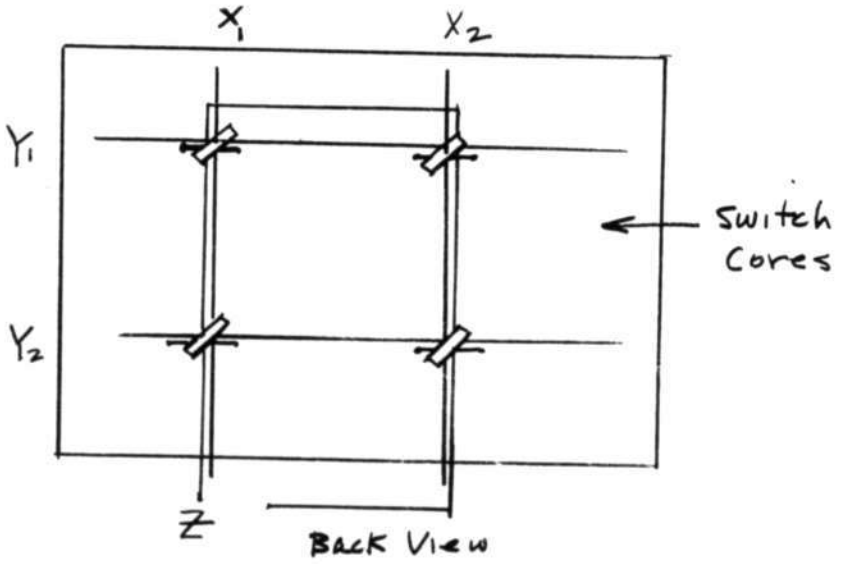



FIG. 3



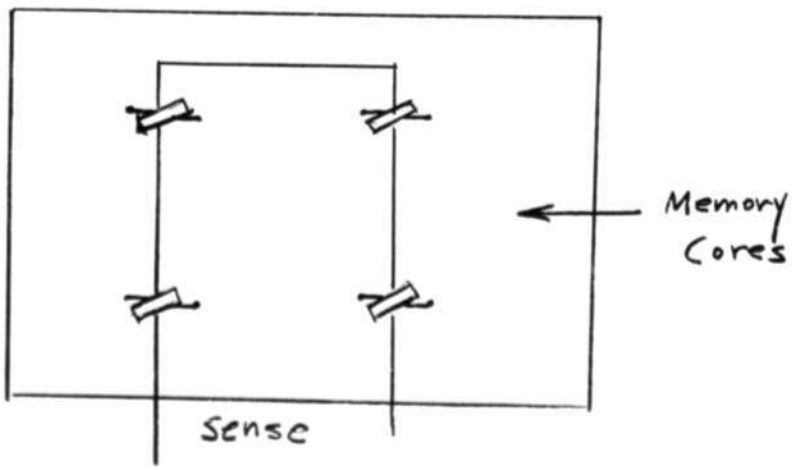




FIG. 4