Division 6 - Lincoln Laboratory
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SUBJECT: HIGH-SPEED CORE DRIVER

To: Group 62 Staff; Group 63 Staff

From: S. Bradspies

Date: October 21, 1954

Approved: W. N. Papian

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Abstract: A high-speed core driver has been developed. The circuit consists of two pulse amplifiers, a slave flip-flop, a buffer amplifier (which has very rapid rise and fall times), and a current amplifier (Fig. 1). The rise and fall times of the output current pulse are approximately 0.05 microsecond. The current pulse output is negative (as in the Mod V core driver) and its amplitude exceeds 1.5 amps (Fig. 8).

Introduction

A memory system in which the cores are switched by very large currents, and therefore very rapidly, is being developed.[1] Work on this system using the Mod V Core Driver has been frustrating, partially due to the relatively slow rise time of this driver, and mainly because of its extremely slow fall time.* It has been found that the cores switch before the current through them has risen to its final value. The result has been the inability to take any quantitative data on the operation of the memory system. The solution may be a driver capable of rising and falling more rapidly than the Mod V driver does.

Fig. 1 shows a block diagram of the core driver. The first pulse is applied to Pulse Amplifier 1, which has two outputs from its three-winding output transformer - one positive and one negative. This sets the slave flip-flop whose output rises as rapidly as the rise time of the applied pulse. The second pulse applied to Pulse Amplifier 2 clears the flip-flop in the same manner. A trapezoidal wave is applied to a buffer amplifier which has the ability to rise and fall rapidly.

*It is necessary to switch the cores both during the rise and fall of the currents.

[1]Superscripts refer to similarly numbered items in the bibliography.

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The low impedance output of the buffer amplifier is used to drive four 6CD6's in parallel. The output is taken from the plates of the 6CD6's and is greater than 1.5 amps in the negative direction; it rises and falls in less than 0.1 microsecond. This current amplifier stage is very much like that found in the Mod V core driver.[2,3]

The outputs of the flip-flop and the buffer amplifier (Figs. 4 and 6) are trapezoidal in order to achieve a rectangular current output. The reason for this situation is the RC combination in the cathodes of the current amplifier tubes (time constant = 0.1 microsecond). If the flip-flop output were rectangular then the current amplifier would have an overshoot (Fig. 9). The RC combination is required to prevent oscillations in the output.

Slave Flip-Flop[4]

The fast operation of the high-speed core driver (Fig. 2) is due to the ability of the slave flip-flop to change states as rapidly as the rise times of the input pulses (for 0.1 microsecond input pulses, the flip-flop can be set in 0.05 microsecond).

In the quiescent condition V2A is on and V2B is off. The output voltage is taken from the plate of V2A, which is normally clamped at -215 volts (in order to hold the current amplifier stage cut off).

The application of a positive 0.1 μsec pulse at input 1 of pulse amplifier 1, results in the application of a positive pulse at point A and a negative pulse at point B (Figs. 1, 2, 3). The diodes, CR4 and V3, pass these pulses and turn V2A off and V2B on rapidly, but only partially. The switching operation finishes slowly by means of the feedback loops. The reason for this peculiar mode of operation has already been explained - - in order to achieve a rectangular current output, the flip-flop output must be trapezoidal.

The waveform at the cathode of V3 (flip-flop output) is shown in Fig. 4 (the d.c. level is -215 volts). The waveform at the plate of CR4 is shown in Fig. 5 (d.c. level is -140 volts). This waveform has a dent in it because the diode's recovery time is not zero (i.e. - some time is required before the crystal diode can switch from the low forward resistance to the high back resistance). A dent such as this could not be tolerated in the output, and so a vacuum diode, V3, rather than a crystal is used. The capacitance from plate and grid to cathode of the 5965 is large compared to that of a germanium diode, however, and this could cause a dent in the output waveform caused by coupling of the pulse's trailing edge (from A) through this capacitance to the output. Two sections in series minimize this effect, and the addition of C15 at their junction helps further to eliminate the dent.

The flip-flop is switched back to its original (steady) state by the application of a positive pulse at input 2 (Figs 3C and D show the pulses at points C and D). In this case, a dent in the output of the flip-flop (Fig. 4) is of no consequence, due to the fact that the current

amplifier stage is well cut off when the flip-flop is down. Thus CR5 may be a germanium rather than a vacuum diode.

The current output is shown in Fig. 8. The amplitude is 1.8 amps and the rise and fall times are each about 0.05 μsec.

The amplitude of the output is controlled by varying the upper clamp voltage of V2A from -150 (maximum output) to -215 (no output). Unfortunately the amplitude control problem is not solved as simply as the above indicates. In order to obtain a rectangular output pulse, the size of the input pulse at point A must be carefully controlled. If the pulse at A is too large, the output appears like Fig. 9; if it is too small, the output is like Fig. 10. The reason for these distorted waveforms follows: The leading edge of the trapezoidal flip-flop output is almost the same height as the pulse at A. The output then approaches the clamp voltage almost linearly. If the slope is too small (pulse at A too large) then the grids of the 6CD6's do not rise as rapidly as their cathodes and, as time progresses, the current output decreases to its steady value (Fig. 9). If the slope is too large (pulse at A too small), then the grids of the 6CD6's rise more rapidly than the cathodes and the current output slowly increases to its final value after the initial jump (Fig. 10). In the ideal case (Fig. 8), the slope of the trapezoid allows the 6CD6 grids to rise just as rapidly as the cathodes rise, resulting in a rectangular output.

Thus, the method of varying the amplitude of the output wave is to observe it and vary both the "amplitude control" (which sets the upper d.c. level of the flip-flop output), and the "input 1 control" (which varies the sizes of the pulses at points A and B).

Fig. 11 shows a 0.1 μsec, 2.1 ampere pulse output from the core driver. This demonstrates the speed with which this circuit operates, for the slave flip-flop has been set and cleared in about 0.1 μsec.

Fig. 12 shows a 1.8 μsec, 1.8 ampere square wave output. This demonstrates the ability of the circuit to hold a fixed output for a relatively long period of time, despite the necessity for using a peculiarly shaped output from the flip-flop.

Buffer Amplifier

The output voltage of the buffer amplifier used in this core driver rises and falls rapidly (Fig. 6). When the flipflop output is down (-215 volts), both the upper and lower tubes (V_4) conduct fairly heavily. The plate waveform of the upper tube is shown in Fig. 7.

Upon the application of the rapidly rising edge of the trapezoidal wave to the grid of the upper tube, a large slug of current is drawn, dropping the plate voltage of the upper tube to about -73 volts (Fig. 7); the lower tube is immediately cut off by the feedback arrangement. This means that all the current drawn is used to charge stray wiring capacity and so the cathode follower output rises rapidly. Following this

there is an increase in bias on the upper tube, and a resulting increase in its plate voltage, turning the lower tube on again, but not heavily. Part of the current now drawn continues to charge the capacity (resulting in the steadily increasing voltage of Fig. 6); the rest flows through the lower tube.

When the input to the buffer amplifier suddenly drops, the upper tube tried to go off, but the following circumstances prevent this from happening. The plate voltage of upper tube rises and this results in a large current flowing through the lower tube, whose grid is capacitatively coupled to the plate of the upper tube. This current discharges the wiring capacity, and so the output of the buffer amplifier is forcibly pulled down. The upper tube cannot turn off completely because its cathode falls almost as fast as its grid does.

The remainder of the circuit, the pulse amplifiers[5] and the current amplifier[2,3], present no material that is not well-known, and so no description is given of their operation.

It is to be noted that all waveforms shown were made using a Tektronix 514 oscilloscope in which the input was taken directly to the vertical deflection plates of the scope.

Signed: Sydney Bradspies
S. Bradspies

SB:jd

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2. Boyd, Harold W., "Core Drivers - Model V and Model VI", MIT Digital Computer Laboratory Engineering Note E-523, February 10, 1953.

3. Childress, J.D., "Core Drivers - Model V and Model VI Applications, Limitations and Modifications", MIT Digital Computer Laboratory Memorandum M-2755, April 1, 1954.

4. Boyd, Harold W., "The Normalized Flip-Flop Chart", MIT Digital Computer Laboratory Report R-227, July 21, 1953, Appendix IV.

5. Pulse Amplifier Model B, Military Reference Data, Section 131, Basic Circuits, MD 112, November 21, 1953.

Memorandum 6M- 3107

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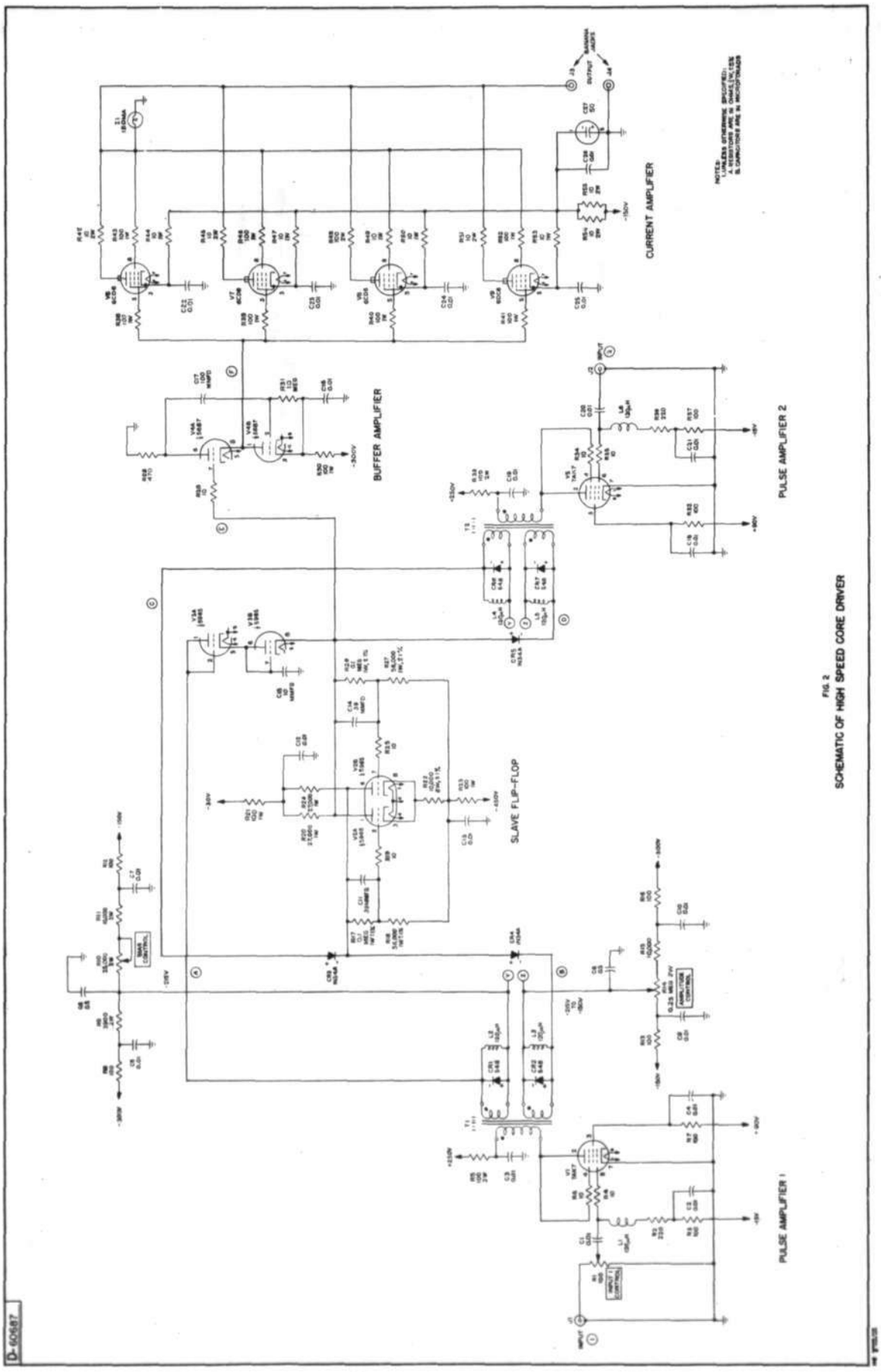

FIG. 2
SCHEMATIC OF HIGH SPEED CORE DRIVER

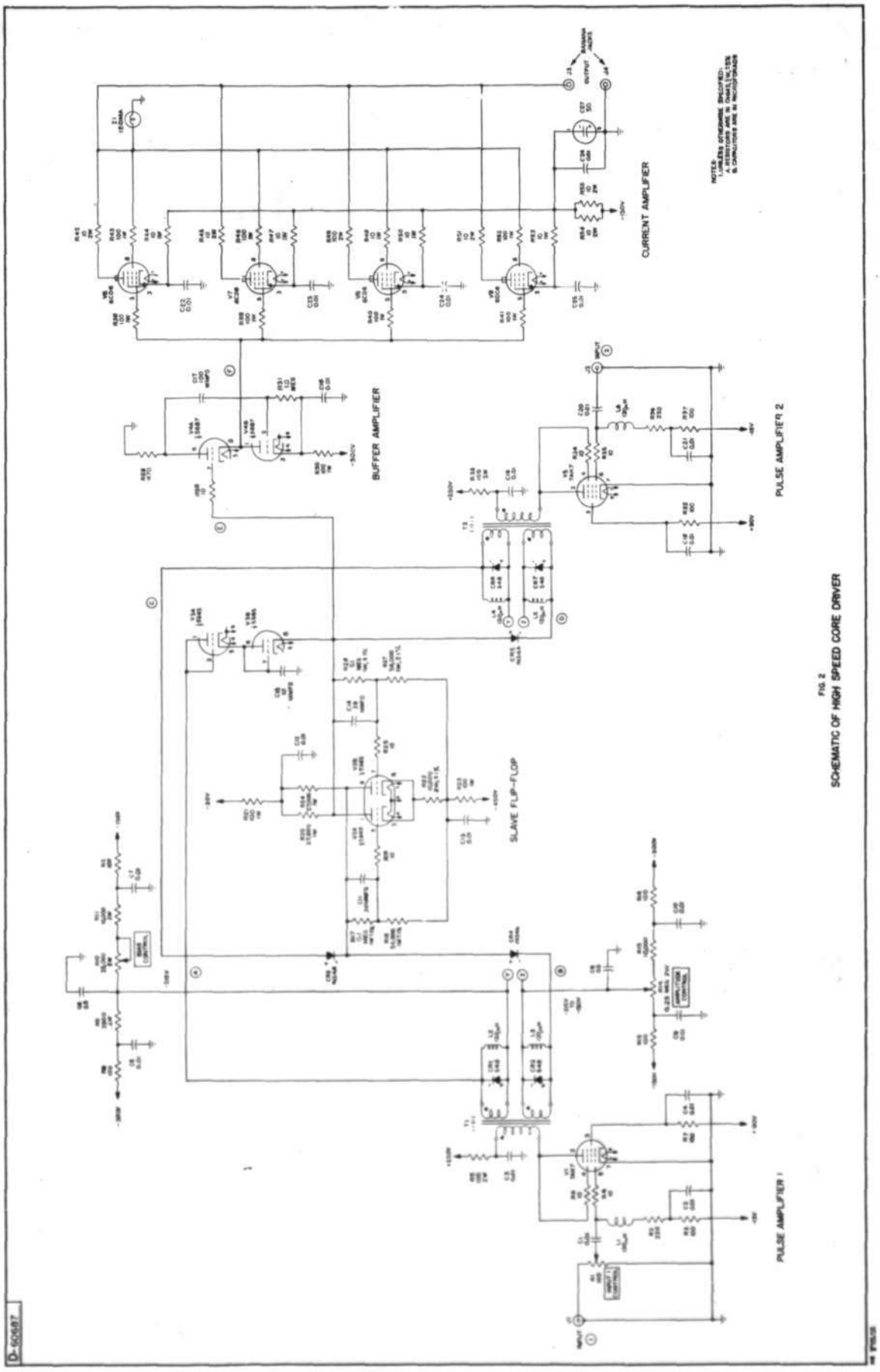

FIG. 2
SCHEMATIC OF HIGH SPEED CORE DRIVER

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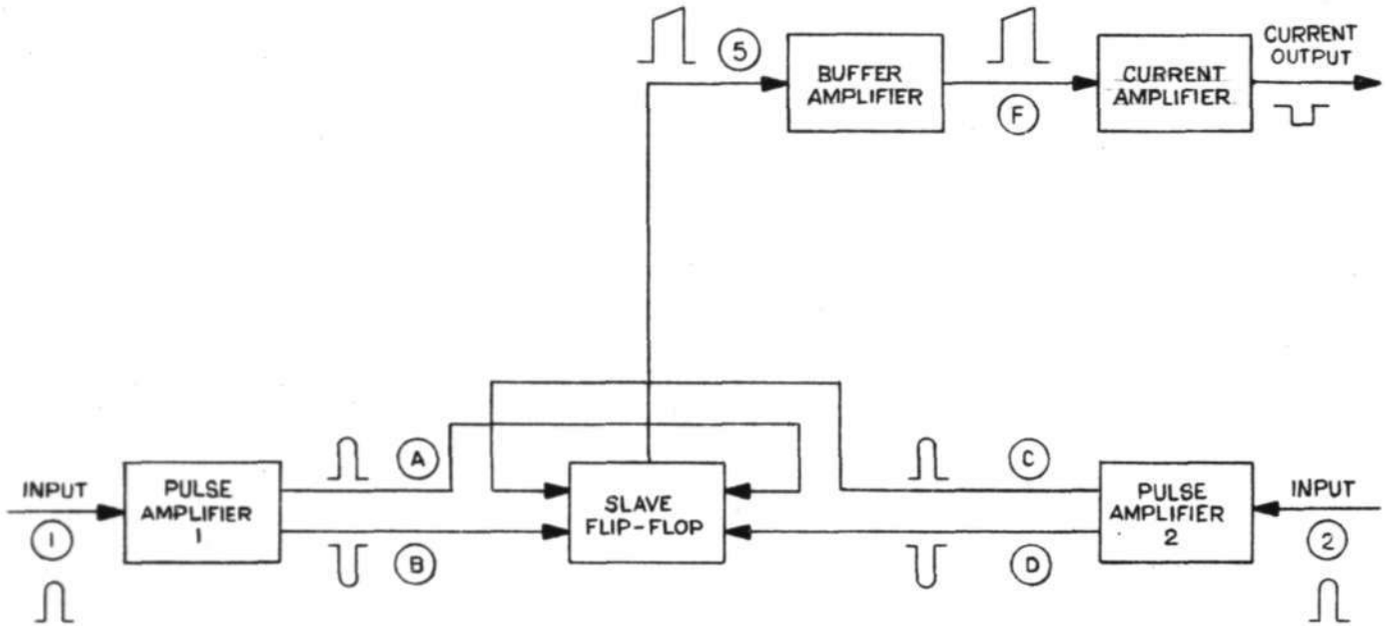


FIG. 1
BLOCK DIAGRAM OF HIGH SPEED CORE DRIVER

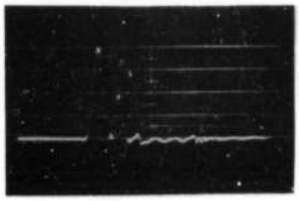


FIG. 3A
VOLTAGE AT POINT A
CORRESPONDING TO FIG. 8

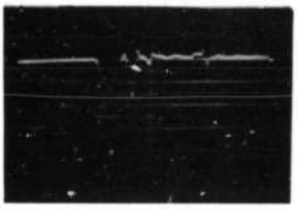


FIG. 3B
VOLTAGE AT POINT B
CORRESPONDING TO FIG. 8

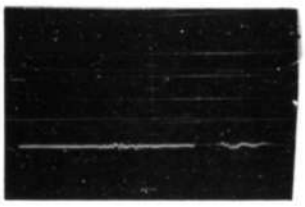


FIG. 3C
VOLTAGE AT POINT C
CORRESPONDING TO FIG. 8

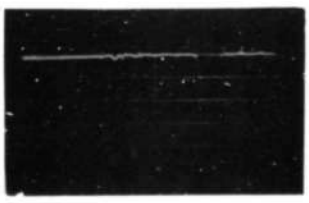
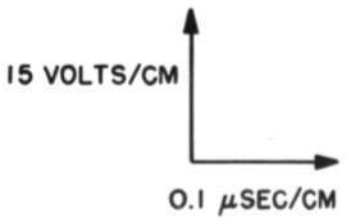


FIG. 3D
VOLTAGE AT POINT D
CORRESPONDING TO FIG. 8



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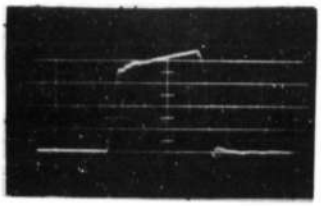


FIG. 4
FLIP-FLOP OUTPUT
(WAVEFORM AT CATHODE OF V3)
CORRESPONDING TO FIG. 8
DC LEVEL=-215 VOLTS

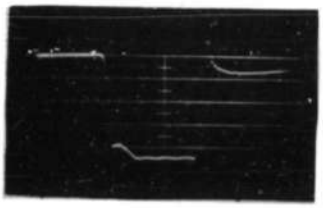


FIG. 5
WAVEFORM AT PLATE OF CR4
CORRESPONDING TO FIG. 8
DC LEVEL=-140 VOLTS

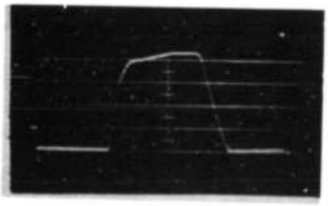


FIG. 6
BUFFER AMPLIFIER OUTPUT
CORRESPONDING TO FIG. 8
DC LEVEL=-210 VOLTS

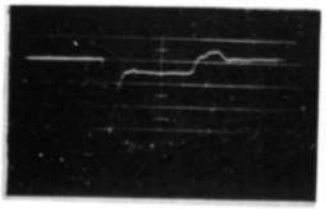
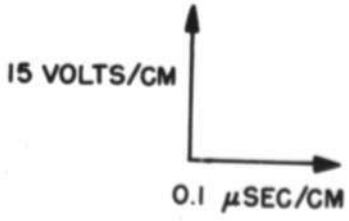


FIG. 7
BUFFER AMPLIFIER PLATE
WAVEFORM
CORRESPONDING TO FIG. 8
DC LEVEL=-27 VOLTS



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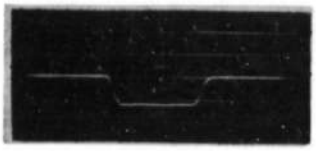


FIG. 8
BEST CORE DRIVER OUTPUT CURRENT (THROUH 10Ω LOAD)

FIG. 9
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO LARGE

FIG. 10
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO SMALL

FIG. 11
0.1μSEC CORE DRIVER OUTPUT CURRENT PULSE

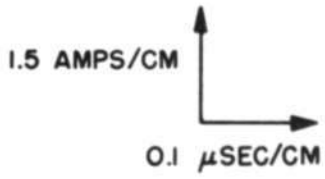
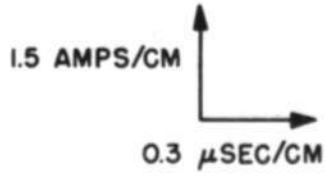


FIG. 12
1.8μ SEC CORE DRIVER OUTPUT PULSE



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