Division 6 - Lincoln Laboratory
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SUBJECT: PROPOSED MEMORY ADDRESS SELECTION SYSTEM

To: N. H. Taylor

From: David Shansky

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Abstract: Increased economy in the use of cathodes is made possible by multi-level memory address selection and improved circuit designs.

In view of the increasing amount of thought being devoted to the possible construction of a 128 x 128 (16384-register) memory it was decided to review the existing memory address-selection system with the hope of reducing the cathode count, easing the driving problem, and decreasing memory cycle time. As a result of this review a driver arrangement has evolved which, along with improved circuit designs, requires fewer cathodes (total) to drive a 128 x 128 memory than are presently being used to drive the 64 x 64 memory.

In terms of actual cathode count, the present 64 x 64 memory requires a total of 1400 cathodes (exclusive of memory control). The proposed arrangement for the 128 x 128 memory requires fewer than 1200 cathodes. The 2 arrangements can be compared as follows. The existing 64 x 64 memory (M.T.C.) uses a 64-position crystal matrix switch and a single gate generator which gates all the cathodes of the selection plane drivers in a given coordinate for a given direction. The XD-I memory uses a 32-position switch (but the same number of cathodes in the matrix output amplifiers and cathode followers which drive the Selection-Plane driver grids) and 2 gate generators, each gating half the cathodes in a given coordinate. The proposed 128 x 128 driver uses a 16-position crystal switch (a 4-input "and" gate) driving the grids of the 5998 driver tubes and 8 gate generators driving the cathodes of these driver tubes. For the purpose of driving the grids of the 5998 selection-plane drivers it is proposed that a matrix-output-amplifier and cathode-follower channel using 7AK7s be developed. The gate generators in the cathodes can simply be digit-plane drivers (new circuit) with 4-input crystal "and" gates. It appears that address selection could be accomplished almost as rapidly as the Flip-Flop transition time at no great strain or expense.

The standby current requirements of the memory are also considerably reduced due to the reduction in number of matrix output amplifiers.

It would seem from the preceding discussion that the optimum arrangement (as far as cathode count is concerned) results when the number of cathodes in the gate generators equals the number of S.P.D grid-driving cathodes.

The preceding estimate of the cathode count assumes 4 cathodes in each gate generator, 4 in each sense amplifier, 5 in the Digit-plane driver, and 2 cathodes in each matrix-output-amplifier and cathode-follower channel. The necessary diode logic can easily be driven by 3 cathodes on each line.

Signed David Shansky
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Approved R L Best
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DS:jb

See Attached Chart

Distribution

Group 62, 63 } Staff

N. L. Daggett

W. Wittenburg (I.B.M.)

| | "64 x 64" Existing System (XD-1) Present CKts | "64 x 64" Existing System (XD-1) Improved CKts | "64 x 64" New System Improved CKts | "128 x 128" Present System Improved CKts | "128 x 128" New System Improved CKts |
|---|---|---|---|---|---|
| M.A.R. C.F. | 216 | 72 | 72 | 84 | 84 |
| M.O.A. | 128 | 64 | 16 Pos. Sw.-32 | 32 Pos. Sw. -64<br>16 Pos. Sw.-32 | 64 Pos Sw.-128 |
| M.O.A. C.F. | 128 | 64 | 32 | 32 Pos. Sw.-64<br>16 Pos. Sw.-32 | 128 |
| Read Write Gate Generator | 48 | 32 | 4 G.G.-64 | 4 G.G. 64<br>8 G.G. 128 | 48 |
| Total, Selection System | 520 | 232 | 200 | 276 | 388 |
| Driver S.P.D. | 256 | 256 | 256 | 512 | 512 |
| Sense Amp. | 363 | 132 | 132 | 231 | 231 |
| Digit Plane Drivers | 251 | 165 | 165 | 165 | 165 |
| Inhibit G.G. | 11 | 4 | 4 | 4 | 4 |
| Total Cathodes | 1401 | 789 | 757 | 1188 | 1300 |