A.D. Hughes

November 12, 1953

MASTER'S THESIS PROPOSAL

TITLE: The Incorporation of a Magnetic Matrix Switch into a Multiplanar Coincident-Current Magnetic Memory.

BRIEF STATEMENT OF THE PROBLEM

The purpose of this thesis is to investigate the problem of driving a large (64 x 64 x 32 digit) coincident-current magnetic-core memory using magnetic switch cores.

HISTORY OF THE PROBLEM UP TO THE PRESENT TIME

Storage of digital information using a three-dimensional array of magnetic cores has been under investigation of the Digital Computer Laboratory of MIT for some time.[1,2] The advantages of such a memory are its compactness, reliability, speed of operation, relative ease of construction, and simplicity. These advantages are confirmed by the recent installation and successful operation in the Whirlwind I computer of a magnetic-core memory consisting of two arrays, each containing 1024 registers and a 17-digit word length.

The storage of binary information requires that each element of memory store either a ONE or a ZERO. The ability of a square-hysteresis-loop magnetic core (a small toroid in this case) to remain indefinitely in one of two stable states lends itself nicely to the storage of binary information. If we call the two remanent states ONE and ZERO, a ONE is "written" into the core by a field produced by a wire carrying current through the core in one direction; a ZERO is written into the core by current in the opposite direction. A ONE or ZERO is "sensed" by writing a ZERO into the core; a third winding detects whether there is a large or a small change in flux.

Since the hysteresis loop of the magnetic core used is square, a current of, say, I_m will "switch" the core from one state to the other, whereas a current of $I_m/2$ will not (see Fig. 1). This feature is used in the Whirlwind system by building up a coincident-current memory array of two-dimensional "planes" and stacking them for the third dimension. A memory plane consists of "x" times "y" cores wired at the intersections of x vertical wires and y horizontal wires. A current of $I_m/2$ through an x and y wire will switch a "selected" core where the two wires intersect but will leave the other cores virtually unchanged. Since the planes are

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1 Superscripts refer to similarly numbered items in the Bibliography.

stacked so that the x and y wires of each plane are in series, an x and y current will select a core in each plane. These selected cores make up a register of "z" digit length, for z planes. To select digits within the register, a z winding in each plane passing through every core carries current -I/2 to inhibit those digits in order to make them ZERO.

There are many possible selection schemes besides the one described above.[3,4] Some use a better selection ratio but usually require more associated equipment. For driving current, in general, vacuum tubes can be used. Whirlwind I, in particular, does use vacuum-tube drivers and crystal diodes for x and y address selection. Vacuum tubes, however, are one of the chief causes of failure in computers. Many systems proposed reduce the number of tubes by using transformers[5] or other devices.[6,7,8] Magnetic cores are particularly promising not only for current drive but for address selection at the same time.

The use of magnetic cores as gates (saturable-core transformers) dates back to the 1900's. Comparatively recently, their use in digital computers was proposed[9,10] and is now being investigated quite extensively. Investigation of a magnetic matrix switch for a coincident-current magnetic-core memory was undertaken by K.H. Olsen and a Master's Thesis written.[6] The Olsen switch consists of 2^n magnetic cores (where n is the number of lines to be driven) with a driving winding and bias windings as shown in Fig. 3. The bias current will drive all but the selected core into saturation, (see Fig. 2). The driver can then only deliver power through the core not biased into saturation. Fairly successful operation of a 16 x 16 memory plane by two 16-position switches was accomplished. When another 16 x 16 plane was added to the first, operation was marginal. It can be seen that when as many as 32 planes are driven, the load on a switch is considerable. Since 1 to 32 cores could be switched, depending on the word stored, the problem of regulation is also involved.

Other considerations interdependent upon current amplitude and regulation are those of pulse shape and width. This adds considerable complexity to the problem. That is, introducing a variable-load effects the pulse shape as well as the amplitude, which directly effects the design of the switch.

PROPOSED PROCEDURE

Introduction

The basic functions to be performed are the address selection and current driving of a memory array. Since the magnetic switch is readily adaptable to the present logical system of address selection and current driving, it was decided to adapt the magnetic-core switch to this system, replacing the x and y address crystal matrix and x and y current drivers. (The alternative was to try entirely different selection and driving schemes.) Even after this basic decision has been made many problems still remain to be solved in driving a large memory.

Since a switch core is not used as a coincident-current device the requirement no longer holds that a current I_m must switch the core and $I_m/2$ must not. Otherwise, the magnetic material used is the same as that used for memory cores. (The actual switch core will be much larger, of course.)

Two types of square-loop magnetic materials suitable for switch cores are available: ferrite (a ceramic material) and thin magnetic metallic ribbon wound on a bobbin. Olsen's first switches were built with ferrite cores. However, when a switch with large enough cores to drive a multiplanar memory was built and tested, the heat generated at operational switching speeds changed the characteristics of the core. Temperature tests by the author showed that metallic cores would not heat so readily and that they could stand a much higher temperature change before their characteristics changed. The amount of net ampere-turns needed to switch a metallic core is much less than for a ferrite core. For these reasons it has been decided to use metallic cores in the switch. Molybdenum-Permalloy 1/4 mil-tape wound on a bobbin has proved a satisfactory core material.

Probable Procedure

Work with single cores will continue in order to produce the proper waveshape, amplitude, and regulation of current for driving the memory. The variables are core geometry, number of turns, load impedance, source impedance, and source waveshape. Work has been done by Olsen, the author, and others[11] on equivalent-circuit techniques; insofar as equivalents help the progress of the switch design, work will continue on their evaluation and use.

After the nature of the desired input to the switch is determined, design of circuits to provide this easily will be investigated. Considerable attention will be given to the bias drivers for the switch. Virtually no attempt has been made to use other switch cores or linear transformers for the bias-current drive.

Experiments with a small switch with a dummy load or equivalent memory load will be completed first. Then a 64-position switch will be built and tested. If time permits and the results up to this point are good, a second switch will be built and a large memory actually driven.

EQUIPMENT NEEDS

All equipment is available at the Digital Computer Laboratory. Standard pulse-test equipment will be used wherever possible. If results are good, the Memory Test Computer at the Laboratory may be used as a final test. Facilities for the construction of any specially designed equipment are also available at the Laboratory.

Magnetic cores are procured from Magnetics, Inc., Butler, Pa., by the Laboratory.

ESTIMATED DIVISION OF TIME

1.	Preparation of Proposal	75 hours
2.	Further Study of Literature	25 hours
3.	Experimental Work and Analysis	150 hours
4.	Correlation of Results and Formulation of Conclusions	75 hours
5.	Preparation of Thesis Report	75 hours
6.	Total	400 hours

SIGNATURE AND DATE

A. D. Hughes

A. D. Hughes

November 12, 1953

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

Approved: William K Linvill

William K. Linvill,
Associate Professor of Electrical Engineering

ADH/cs

Drawing Attached:

B-50910

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5. F. Durgin, E. Gates, "First Note On Pulse Transformers for Memory Drivers," Digital Computer Laboratory Memorandum M-1987 (May 27, 1953).

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10. J.G. Miles, "Saturable Core Reactors as Digital Computer Elements," A Report of the Engineering Research Associates (June 17, 1949).

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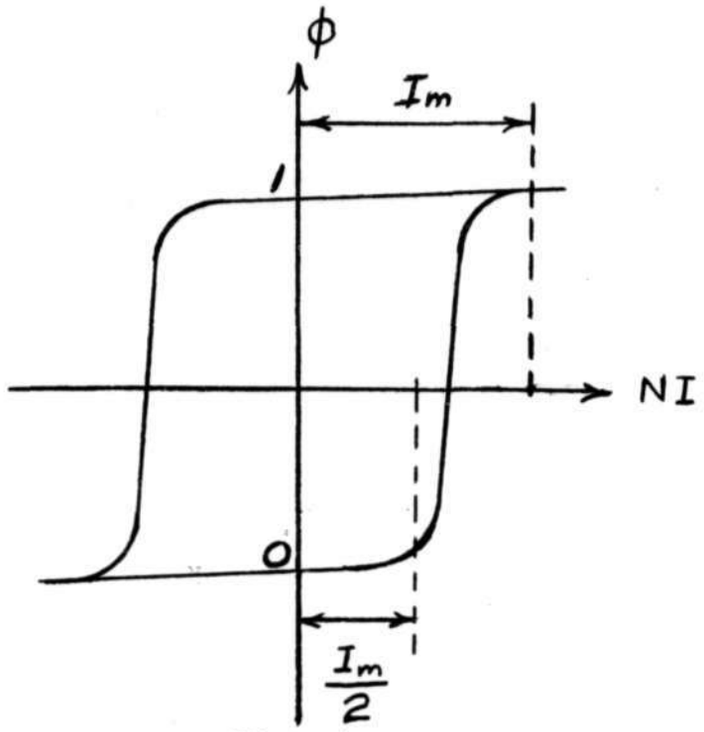


FIG. 1

Memory Core Hysteresis Loop

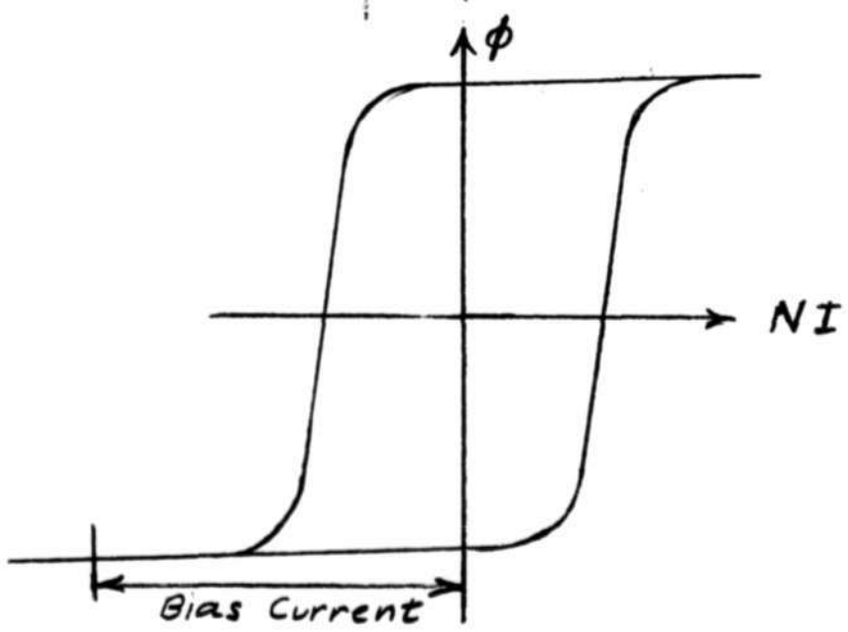
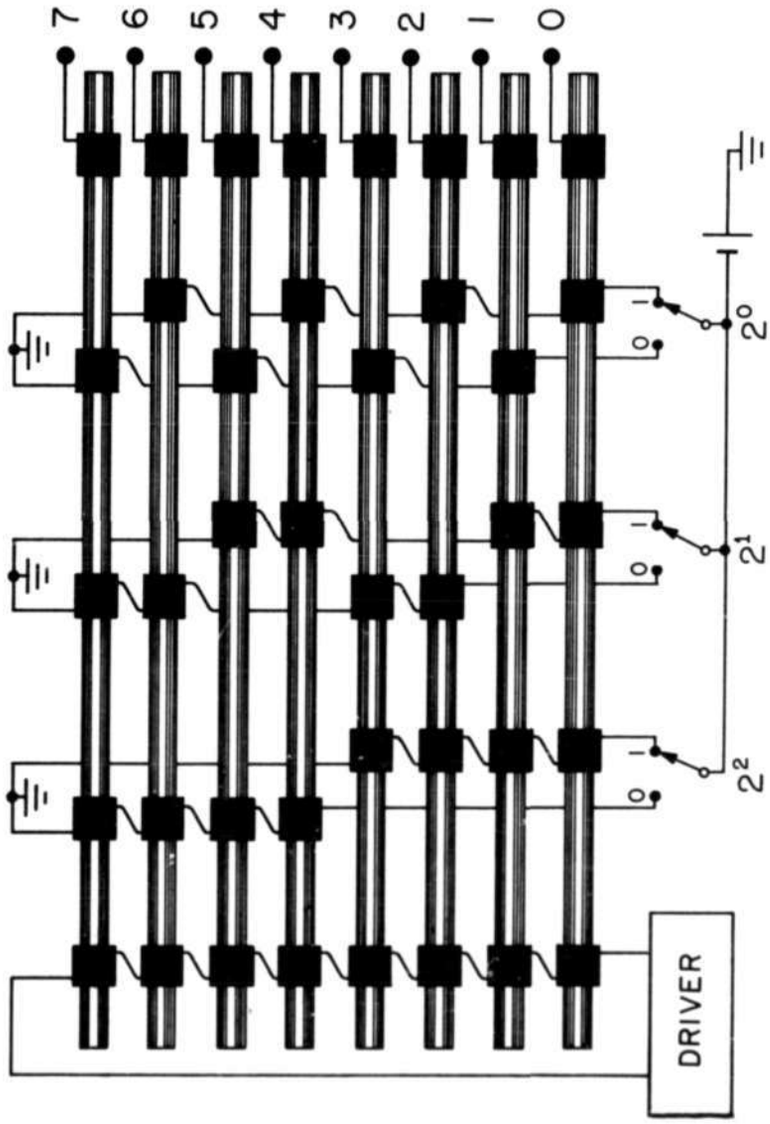


FIG. 2

Switch Core Hysteresis Loop



8-POSITION MAGNETIC-MATRIX SWITCH

FIG. 3

B-5090
F-1470
SN-372