Division VI - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SENSING WINDING GEOMETRY

To: N. H. Taylor

From: J. Raffel

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Abstract: The difference between the minimum wanted output (a system ONE) and the maximum unwanted output (a system ZERO) is the same for a winding which threads the cores so that each half of the memory plane has a different polarity as it is for one in which all the outputs add.

Introduction

This memorandum concerns itself with the analysis of the signal and noise in the present sensing winding and in a proposed winding, and will not consider other associated factors such as plane construction, sense amplifier design, etc.

Present Sensing Winding

When the first magnetic memory planes were being designed, before any detailed work had been done to determine the exact nature of the half-selected outputs which might appear in an array, the assumption was made that these voltages were approximately uniform and independent of the previous history of the core. This led quite naturally to a sensing winding geometry which tended to have the half-selected outputs cancel. This was accomplished by having the winding thread the cores in a diagonal fashion so that cores in two halves of the plane were threaded in opposite directions. The wiring scheme is shown in Figure 1. With this type of winding it turns out that all but two half-selected outputs are of canceling polarities.

Since the construction of these first planes a good deal of information has been obtained about the types of half-selected outputs which can appear on the sense winding. The original assumption of equal outputs from all half-selected cores is no longer justified. It is logical therefore to reconsider the problem of sensing winding geometry. The term "canceling" will be used to describe the present winding and "additive" will be used to describe that proposed which will thread the cores in such a way that all the outputs appear with the same polarity on the winding.

The following definitions will be used below:
(All definitions are for values at stroke time)

h_1 the maximum output possible from a half-selected core.

h_0 the minimum output possible from a half-selected core.

s_1 the minimum output from a selected core containing a ONE.

s_0 the maximum output from a selected core containing a ZERO.

$ZERO_{max}$ the maximum sensing winding voltage when a core containing a ZERO is selected.

ONE_{min} the minimum sensing winding voltage when a core containing a ONE is selected.

$\delta = (h_1 - h_0)$

$D = ONE_{min} - ZERO_{max}$

For an nxn memory containing n^2 cores the following results may be seen to hold:

Canceling

$ONE_{min} = s_1 - 2h_1 - (n-2)\delta$

$ZERO_{max} = s_0 - 2h_z + (n-2)\delta$

$D = s_1 - s_0 - 2(n-1)\delta$

For additive

$ONE_{min} = s_1 + 2(n-1)h_z$

$ZERO_{max} = s_0 + 2(n-1)h_1$

$D = s_1 - s_0 - 2(n-1)\delta$

The difference between the minimum wanted output and the maximum unwanted output is the usable signal, D. Since this difference is seen to be the same for the two systems, it would seem that a re-evaluation of the canceling winding is needed to determine if it really buys anything, especially since plane construction and amplifier design are affected so strongly by the sensing winding geometry.

Signed: J. Raffel
J. Raffel

Approved: WNP
W. N. Papian

JR/rb

cc: Group 63 - Staff
A. P. Kromer - (IBM)
Magnetic Memory Section - Staff

Drawing: A-51628

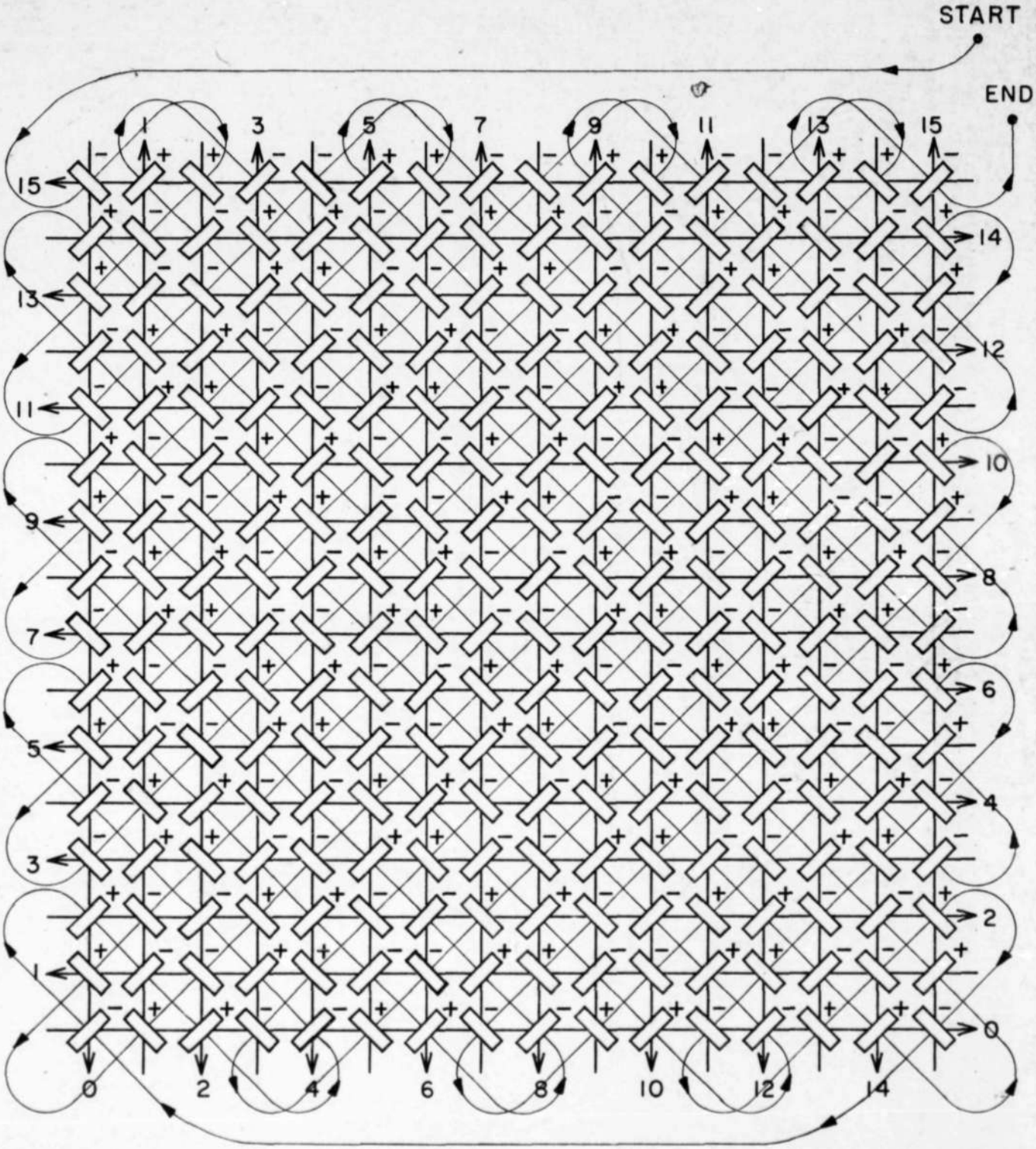

FIG. 1

WINDING GEOMETRY-CERAMIC ARRAY #1

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