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SUBJECT: PULSE RESPONSE OF FERRITE MEMORY CORES

To: Group 63 Staff and Memory Section Staff (Group 62)

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Abstract: The fourteen basic pulsed voltage outputs of ferrite memory cores are defined and discussed. Photographs are presented. The distinctive appearances of certain outputs are noted. The concept of reversible and irreversible outputs is explained and its application is used in understanding the post-write disturbed method of operating a memory. The principle of operation of a magnetic-core memory is described in order to indicate what sequence of pulses are possible in an array. Based on core response only, the most adverse possible outputs of a plane are presented. Estimates of these outputs for MF-1326-B, F-394, cores are made. Typical values for the various core voltage outputs of MF-1326-B, F-394, are given for a driving force of 0.82 amp-turns.

Introduction

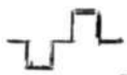
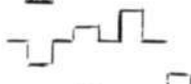
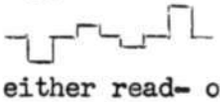
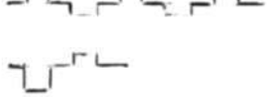
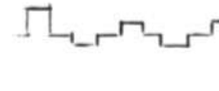
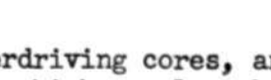
The voltage output of a ferrite memory core depends on the following things: (1) the kind of driving pulse it receives (i.e., fully-selecting or half-selecting); (2) the information the core holds (i.e., ONE or ZERO); and (3) the sequence of half-amplitude disturbing pulses that has preceded the selecting pulse in question. Selecting pulses are always READ polarity pulses. Fundamentally, the disturbing pulses that have preceded a given selecting pulse will either leave the magnetic state of a core undisturbed or in one of two slightly modified states. A core in one of the modified magnetic states is said to be a disturbed core. Figure 1 identifies the seven fundamental magnetic states with respect to the hysteresis loop. A remanent magnetic state is identified by a symbol which is the subscript of the symbol for the corresponding fully-selected voltage output obtained from that state. The output voltage symbols are given in Table I. The disturbed states are referred to as write-disturbed or read-disturbed depending on whether the last disturbing pulse preceding the selecting pulse was a half-amplitude WRITE pulse or a half-amplitude READ pulse respectively. It will be noted from Figure 1 that half-amplitude WRITE pulses alone will not disturb a core holding an undisturbed ONE. Also, analogously, half-amplitude READ pulses will not disturb a core in the undisturbed ZERO state.

Pulsed Voltage Outputs

Many distinct voltage outputs are possible, but basically only fourteen kinds exist.* The output of a core depends on the magnetic state of the core and whether the core receives a full- or half-amplitude selecting pulse. Table I lists these outputs by name and symbol, and indicates the simplest series of pulses which will produce them. The last pulse of each sequence is the selecting pulse.

Table I

Pulsed Voltage Outputs of Magnetic Memory Cores

Name	Symbol	Pulse Sequence (READ pulses up, WRITE pulses down)
Undisturbed ONE	u^{v}_{1}	
Read-disturbed ONE	r^{v}_{1}	
Write-disturbed ONE	w^{v}_{1}	
Disturbed ONE	d^{v}_{1}	either read- or write-disturbed ONE**
Undisturbed ZERO	u^{v}_{z}	
Disturbed ZERO	d^{v}_{z}	
Read-disturbed ZERO	r^{v}_{z}	
Write-disturbed ZERO	w^{v}_{z}	
Undisturbed half-selected ONE	u^{v}_{hl}	
Read-disturbed half-selected ONE	r^{v}_{hl}	
Write-disturbed half-selected ONE	w^{v}_{hl}	
Undisturbed half-selected ZERO	u^{v}_{hz}	
Disturbed half-selected ZERO	d^{v}_{hz}	
Read-disturbed half-selected ZERO	r^{v}_{hz}	
Write-disturbed half-selected ZERO	w^{v}_{hz}	

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* Use of very short duration driving pulses, overdriving cores, and other such conditions give rise to output variations which are less basic in nature than those discussed here. All such observed outputs may be classified as special cases of the basic fourteen outputs.

** See section on Fully-Selected ONE outputs.

Fully-Selected ONE Outputs (Figure 2)

The undisturbed ONE output is distinct from the two disturbed ONE outputs. The characteristics of the undisturbed ONE have been reported previously and require no discussion here. The two disturbed ONE outputs are identical except for the difference in amplitude of the "spike" at the beginning of the pulses, the write-disturbed ONE having the higher spike. Because the values of the write-disturbed ONE and the read-disturbed ONE voltages at and near the strobe time are equal,* and the value of the switching time is not affected by variations in the disturbing mode, it is not generally necessary to differentiate between the two outputs. Since for most considerations, the read-disturbed ONE and the write-disturbed ONE may be considered identical they are usually not distinquished between and are simply referred to as the disturbed ONE output symbol $_{d}V_{1}$.**

Fully-Selected ZERO Outputs (Figure 3)

The undisturbed ZERO output is the smallest of the fully-selected ZERO outputs. It is different from all other fully-selected outputs in that it is the result of a reversible magnetization change, i.e. the remanent magnetic state of the core is not altered by the selecting pulse. Such pulses are referred to as reversible, as opposed to irreversible for those which accompany a change in the magnetic state of the core.

The read-disturbed ZERO is characterized by a distinctive double peak which can be seen in Figure 3. The read-disturbed ZERO is of interest because, although it has a peak amplitude considerably smaller than the write-disturbed ZERO, it has an appreciably slower decay time and therefore is the largest fully-selected ZERO output at strobe time.

The disturbed-ZERO output is closely related to the write-disturbed ZERO output. It is the ZERO output obtained from a core in a memory which has not been otherwise disturbed since writing. An explanation of why this is so is presented in the section on Memory Plane Operation. Figure 3 shows that the disturbed-ZERO is a distinct output slightly greater in amplitude than the write-disturbed ZERO outputs. A similar difference is observed between the disturbed half-selected ZERO and the write-disturbed half-selected ZERO outputs.

Half-Selected ONE Outputs (Figure 4)

The three kinds of half-selected ONE outputs are shown in the composite photograph of Figure 4. The two larger outputs are the undisturbed half-selected ONE and the write-disturbed half-selected ONE respectively. They are irreversible. The read-disturbed half-selected

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* The strobe time is the time at which a core voltage output is sensed in the memory. It is approximately the time of the peak disturbed ONE. See section "Analysis of Memory Plane Output.

** See Table I

ONE is reversible and is the only half-selected ONE output obtained from a memory which uses the post-write disturbing method of operation.

Half-Selected ZERO Outputs (Figure 5)

There are four different half-selected ZERO outputs. The disturbed half-selected ZERO is the largest half-selected ZERO output. It is not shown in Figure 5, but as in the case of the fully-selected ZERO outputs, it is slightly larger than the write-disturbed half-selected ZERO output which is shown. Both the disturbed half-selected ZERO and the write-disturbed half-selected ZERO outputs are irreversible. The undisturbed half-selected ZERO and the read-disturbed half-selected ZERO outputs are reversible. The read-disturbed half-selected ZERO is the only half-selected ZERO output obtained from a memory which uses the post-write disturbing method of operation. It is larger than the undisturbed half-selected ZERO which cannot be obtained from a memory. Neither the undisturbed half-selected ZERO nor the undisturbed fully selected ZERO is ever realized in actual memory operation. The reason for this is explained in the section, "Memory Plane Operation."

Memory Plane Operation Without Post-Write Disturbs

In a coincident-current memory such as is used in the M.I.T. Memory Test Computer, and in Whirlwind I, certain pulse outputs are of greater interest than others. Before discussing the effects of the various pulse outputs on memory operation, it is necessary to consider the mode of operation involved in a coincident-current memory of the MTC type. A core is selected by passing current pulses along two lines corresponding to the row and column of the addressed core, each of the two lines supplying a half-amplitude pulse. All cores on the same row or column as the selected core, therefore, receive half-amplitude pulses. These cores are referred to as half-selected cores. The cores which are neither being selected nor half-selected are called unselected cores. In selecting a core, a READ pulse followed by a WRITE pulse is used. The WRITE pulse will leave a ONE in the selected core. If it is desired to leave a ZERO in the selected core, an inhibiting half-READ pulse is supplied simultaneously with the WRITE pulse resulting in a net half-WRITE pulse. Therefore a ZERO is written into a core by pulsing it with a full-READ followed by a half-WRITE pulse. The inhibiting half-READ pulse is supplied by the digit plane winding which links all cores in the memory plane.

On the basis of the mode of operation described above, Table II presents the various possible pulses to which a core in a memory may be subjected.

Table II

Sequence of Pulses Received by Cores in a Memory Plane
Not Using The Post-Write Disturb

If core in question is:	Information held by the selected core	
	ONE	ZERO
Selected	READ, WRITE	READ, HALF-WRITE
Half-selected	HALF-READ, HALF-WRITE	HALF-READ, NO PULSE
Unselected	NO PULSE, NO PULSE	NO PULSE, HALF-READ

Theoretically, a core may be selected, half-selected, and unselected in any sequence. A study of Table II from this point of view will indicate the possible sequence of pulses a core may experience. It will be noticed that READ pulses are always followed by either WRITE or half-WRITE pulses. For this reason neither the undisturbed ZERO nor the undisturbed half-selected ZERO can ever occur.

As mentioned in the section, "Fully-Selected ZERO Outputs," the disturbed-ZERO is distinct from the write-disturbed ZERO. Table II indicates why the disturbed-ZERO is the ZERO output obtained from a core which has not been disturbed since writing.

Analysis of Memory Plane Output

Consider a memory plane consisting of a square array of n^2 cores. The sense winding from which the plane output voltage is taken passes through all cores. When a particular core is selected for READ-out by pulsing it with a full-READ pulse, all cores on the same row or column as the selected core are also pulsed, but with half-amplitude pulses. The resulting output voltage is the sum of the selected core output plus the half-selected outputs of the 2(n-1) half-selected cores. In order to distinguish between a read-out of ONE and a read-out of ZERO, it is necessary that the largest possible ZERO read-out of the plane not be sufficiently large to be confused with a ONE read-out. In order to minimize the effect of the half-selected outputs on the read-out voltage of the selected core, the sense winding is passed through the cores of the plane in a manner which results in core voltage outputs of alternate polarities on the sensing winding. By this means the net output voltage of a plane is composed of the selected core output minus two half-selected outputs plus the net output of the remaining half-selected cores which tend to cancel one another. This latter output is referred to as the delta voltage. An equation expressing the output of such a memory plane may be written as follows:

$$V_{out} = V_{selected} - 2V_{half\text{-}selected} \pm (n-2)\, V_{delta} \qquad (1)$$

where V_{out} = the read-out voltage of the plane

$V_{selected}$ = the voltage output of the selected core

$V_{half\text{-}selected}$ = the average core voltage output of the half-selected cores whose output polarities on the sensing winding are opposite to that of the selected core.

and V_{delta} = the difference between the average voltage output of the half-selected cores whose polsrities on the sensing winding are the same as that of the selected core and the average voltage output of the half-selected cores whose polarities on the sensing winding are opposite to that of the selected core.

Since it is necessary to discern all possible ONE read-outs from all possible ZERO read-outs, a comparison of the lowest possible ONE read-out with the largest possible ZERO read-out yields a figure of merit for a memory plane. The ratio of the largest possible ZERO read-out to the smallest possible ONE read-out is called the convergence ratio. In order to obtain the most favorable convergence ratio, the amplified output of the plane is gated at approximately the time of the peak disturbed ONE. This time is called the strobe time and the strobe time values of the outputs are the significant ones in Equation 1. Since the delta voltage may be either positive or negative with respect to the output of the selected core, the maximum absolute value of delta voltage is always the one which yields the most adverse output and therefore is the one of interest in evaluating cores for a memory. The minimum possible ONE-out of a memory can be shown to be

$$\pm \left[{}_{d}V_{1} - 2\, {}_{w}V_{hl} - (n-2)\, {}_{wr}V_{d} \right] \qquad (2)$$

and the maximum possible ZERO-out may occur as either

$$\pm \left[{}_{d}V_{z} - 2\, {}_{w}V_{hl} - (n-2)\, {}_{wr}V_{d} \right] \qquad (3)$$

or

$$\pm \left[{}_{r}V_{z} - 2\, {}_{r}V_{hz} + (n-2)\, {}_{wr}V_{d} \right] \qquad (4)$$

where $${}_{wr}V_{d} = {}_{w}V_{hl} - {}_{r}V_{hz}. \qquad (5)$$

The difference between the outputs represented by Equations 3 and 4 is insignificant.

In order to obtain these worst possible outputs, it is necessary to address the memory in a particular sequence. However, it should be remembered that the orders for such addresses come from the memory itself. For this reason, it is obvious that other constraints exist which may make this output pessimistic. Notwithstanding this fact, the output is possible and becomes more probable as the versatility of a machine is increased by collateral storage such as multiple banks and magnetic drums, as is the case with Whirlwind.

Post-Write Disturbed Operation

The post-write disturbed method of operation provides a half-READ pulse to all cores after each memory operation. The half-READ pulse is supplied by the digit plane driver. The sequence of operation, then, is READ, WRITE, read-DISTURB. The effect of the post-write disturbing pulse is to leave all cores in read-disturbed states, and since read-disturbed cores yield reversible outputs, all cores yield only read-disturbed outputs regardless of the sequence of pulsing they have experienced. When using post-write disturbing pulses, Equation 2 becomes

$$\pm \left[{}_{r}V_{1} - 2\,{}_{r}V_{hl} - (n-2)\,{}_{r}V_{d} \right] \qquad (6)$$

and Equation 4 becomes

$$\pm \left[{}_{r}V_{z} - 2\,{}_{r}V_{hz} + (n-2)\,{}_{r}V_{d} \right] \qquad (7)$$

where

$$ {}_{r}V_{d} = {}_{r}V_{hl} - {}_{r}V_{hz} \qquad (8)$$

These are the most adverse read-outs possible using the post-write disturb method of operation. The well-known complemented double-checker board program generates these outputs.

Evaluation of MF-1326-B, F-394, Ferrite Cores for Memory Use

Table III is a list of typical values of voltage outputs from MF-1326-B, F-394 ferrite cores. These are the type used in Bank A of Whirlwind I. The Whirlwind memory is a 32 x 32 memory which uses the post-write disturb. On the basis of the values given in Table III the convergence ratio, which is the ratio of Equation 7 to Equation 6, is 0.9/113 or approximately one percent at strobe time. This should be the value for Whirlwind Bank A. Without the post-write disturb the convergence ratio, i.e. the ratio of Equation 4 to Equation 2, yields

the value 1.8/112 or approximately two percent. With a 64 x 64 memory such as MTC II, the convergence ratio with post-write disturb is 1.9/112 or approximately two percent, and without post-write disturb 3.7/100 or approximately four percent.

Table III

Pulsed Voltage Outputs of MF-1326-B, F-394, Ferrite Memory Cores

(820 ma driving pulse: 2.0 μs duration
0.2 μs rise time) Temperature, 30° C

Peak Values	Symbol	Voltage in Millivolts
Peak undisturbed ONE	$_{pu}V_1$	114
Peak disturbed ONE	$_{pd}V_1$	109
Peak disturbed ZERO	$_{pd}V_z$	19.8
Peak read-disturbed ZERO	$_{pr}V_z$	12.3
Peak undisturbed half-selected ONE	$_{pu}V_{hl}$	8.7
Peak disturbed half-selected ZERO	$_{pd}V_{hz}$	7.2
Peak write-disturbed half-selected ONE	$_{pw}V_{hl}$	6.4
Peak write-disturbed half-selected ZERO	$_{pw}V_{hz}$	6.1
Peak read-disturbed half-selected ONE	$_{pr}V_{hl}$	5.1
Peak read-disturbed half-selected ZERO	$_{pr}V_{hz}$	4.7
Strobe-time Values		
Read-disturbed ZERO	$_{r}V_z$	0.2
Write-disturbed half-selected ONE	$_{w}V_{hl}$	0.1
Write-disturbed half-selected ZERO	$_{w}V_{hz}$	0.1
Read-disturbed half-selected ONE	$_{r}V_{hl}$	0.1
Read-disturbed half-selected ZERO	$_{r}V_{hz}$	0.1
Write-read-disturbed DELTA	$_{wr}V_d = {}_{w}V_{hl} - {}_{r}V_{hz}$	0.06
Read-disturbed DELTA	$_{r}V_d = {}_{r}V_{hl} - {}_{r}V_{hz}$	0.03

From these computations it appears as though MF-1326-B, F-394, cores afford an ample margin for operation in a 32 x 32 or even in a 64 x 64 memory at 820 milliamperes. 820 milliamperes is considered the optimum operating point. The margins of operation become considerably smaller and more difficult to predict at driving forces above 900 milliamperes or below 740 milliamperes. Also, shorter driving pulses or slower rise times will affect the discrimination ratio adversely as will excessive increases in temperature.

Conclusions

1. Ferrite cores used for magnetic memories have fourteen different fundamental outputs: three fully-selected ONE's, three half-selected ONE's, four fully-selected ZERO's, and four half-selected ZERO's.

2. Except for the voltage spike at the beginning of the pulse, the write-disturbed and read-disturbed fully-selected ONE's are identical.

3. Core voltage outputs may be classified as irreversible or reversible depending upon whether the state of the magnetization of the core is changed or not. The post-write disturbed method of operation takes advantage of reversible outputs.

4. The first write-disturbed ZERO output, called disturbed ZERO, is distinctly different from subsequent write-disturbed ZERO outputs. The half-selected ZERO also exhibits this property.

5. The read-disturbed ZERO has a characteristically double peaked output which distinghishes it from other similar outputs.

6. Undisturbed ZERO outputs either fully- or half-selected are not realized in MTC type memory systems.

7. The most adverse read-outs possible from a memory plane when the post-write disturb method of operation is used is obtained from the complemented double checker board program. Based on MF-1326-B, F-394, core outputs alone, the convergence ratio for a 32 x 32 array is approximately one percent with 820 milliamperes driving current. For a 64 x 64 array the convergence ratio is approximately two percent.

8. The most adverse read-outs possible from a memory plane not using the post-write disturb method of operation is not obtainable from the complemented double checker board program but is considerably more difficult to obtain. Considerable flexibility in addressing the memory is required to realize this worst output. Based only on MF-1326-B, F-394 core outputs the convergence ratio for a 32 x 32 array is approximately two percent with 820 milliamperes driving current. The convergence ratio is approximately four percent for a 64 x 64 array.

9. The convergence ratio is affected adversely by slower rise times, shorter driving pulses, or increases in temperature, as well as from departures from the optimum driving current.

Signed James R. Freeman
J. R. Freeman

Approved DRB
D. R. Brown

JRF/jk

Drawings Attached:

Figure 1 A-57238
Figures 2, 3, 4, 5 A-57237

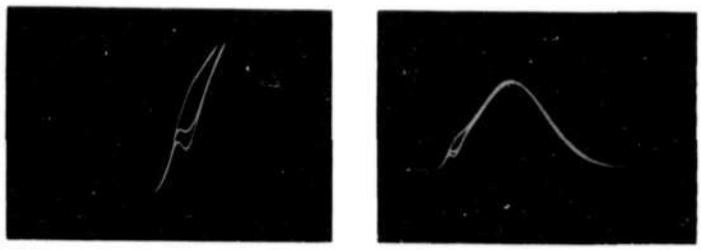

FIG. 2
FULLY SELECTED ONE OUTPUTS

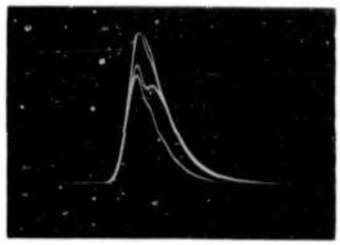

FIG. 3
FULLY SELECTED ZERO OUTPUTS

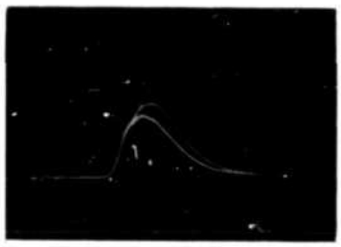

FIG. 4
HALF SELECTED ONE OUTPUTS

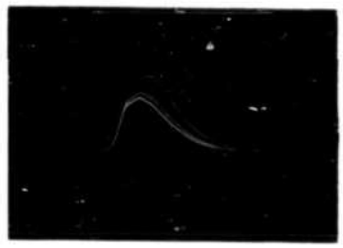

FIG. 5
HALF SELECTED ZERO OUTPUTS
(dVhz NOT SHOWN)

NOTE:
FIGURES 3, 4 & 5 ARE TO THE SAME SCALE

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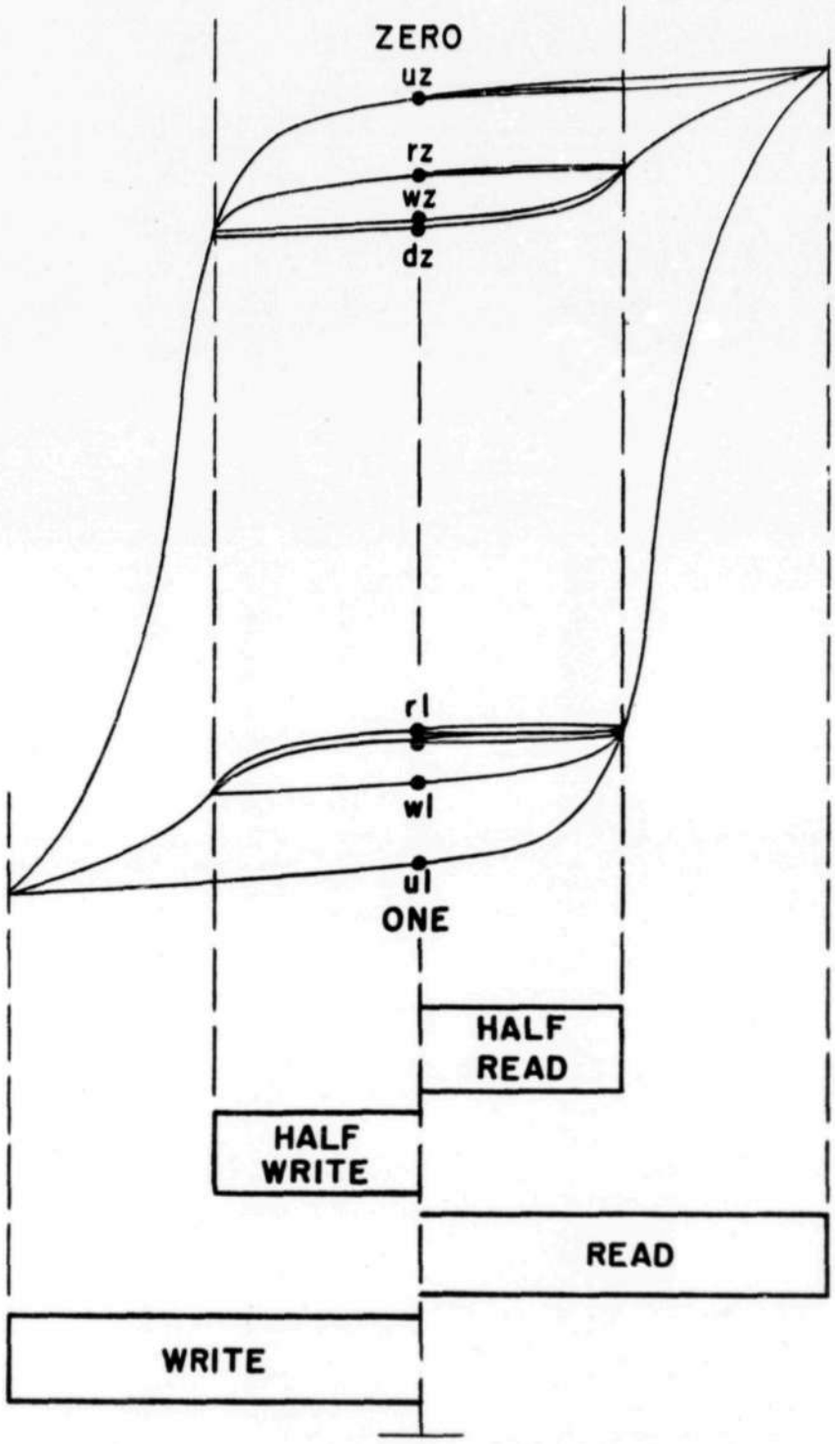

FIG. 1

HYSTERESIS LOOPS ASSOCIATED WITH MAGNETIC MEMORY CORE OPERATION

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