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Memorandum M-1432

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF MARCH 21, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. P. Mayer

Date: March 25, 1952

Members Present:

C. Adams	J. Forrester	W. Linvill	K. Olsen
G. Briggs	W. Hosier	R. Mayer	W. Papian
R. Everett	J. Jacobs	J. O'Brien	C. Schultz
H. Fahnestock	R. Jeffrey	W. Ogden	N. Taylor

The prototype computer will now be called WWIA instead of WWI½.

Rather than talking about generalities, it would probably be a good idea if we concentrated more specifically on WWIA. To review the conclusions so far, the memory will have 1,024 words, each 16 bits long, with ferrite cores driven by a magnetic switch. No further discussion seems necessary on these points unless W. Papian discloses unforeseen difficulties. For the moment we should consider the arithmetic element to be made of transistors with diode gates, but if cores look more promising, we might decide to use them. The control element requires considerably more discussion, so perhaps we should get a few definite ideas to choose from. It seems certain that the control system must distribute energy to different places at different times in order to do an instruction. The approaches suggested so far include the following:

1) The WWI approach using tubes.

2) The WWI approach using cores as gates (in the control matrix).

3) Other ideas using cores.

4) The delay-line approach (referred to as "domino" in the previous meeting).

The above approaches were outlined as follows:

A) The WWI approach using tubes can be found in any of the current WWI literature and makes use of a control switch, a control matrix and a TPD (all of which use crystal diodes). This would probably be the quickest way because it makes use of WWI experience, and the tubes can be electrically matched to transistor and ferrite circuits.

B) The WWI approach using cores was discussed by K. Olsen. In this system, the crystals of the WWI-type control matrix would be replaced by cores using a square hysteresis loop. The control switch would bias off all but one set of these cores. The time pulses would then switch the cores which are not biased off. The sensing winding for each individual command could run through as many of these cores as desired, thus allowing any command to occur on any time pulse of any instruction. Thus no gate tubes nor mixing circuits are required. It is possible to build such an arrangement with 256 cores, one at each junction of the 32 operation lines and the 8 time pulse lines, but it is necessary to put cores only at the useful junctions, and it is even possible to use one core for several junctions in some cases. It would probably be necessary to amplify each command pulse by a Class C amplifier so that when the cores are cleared - (which happens when the control switch is cleared) - the resulting pulse will not appear as a command. Even with these amplifiers, this system saves all the gates and crystals of the WWI system and has only one amplifier per command instead of several.

J. Forrester suggested that the Bell Laboratory Mark VI computer should be investigated because it uses a technique of threading wires through magnetic cores.

It would probably be desirable to allow each operation to have as many time pulses as it requires. This can be done by allowing the completion of the operation to reset TPD to zero.

When resetting the cores, it is necessary to switch several cores on the same line at once. The question was raised whether this introduces an undesirable delay. The answer appears to be that any such delay is in the neighborhood of a few tenths of a microsecond. If this delay becomes objectionable, perhaps logical design can avoid the difficulty.

Everett has suggested that the return path of a line threaded through a string of cores could be woven on the cores in the opposite direction so that each core would have effectively two turns, and flux cancellation would result outside the cores.

C) The delay-line approach was described by Taylor. The control switch (probably a magnetic switch) would select one of several delay lines and would pulse it. The delay line would be tapped at several points so that pulses could be supplied from the delay line to the computer as commands at different times. Fewer tubes would be used in this system than are used in the WWI system. Of course, it would not be convenient to stop an operation once it has started, but experience with WWI indicates that it is not necessary to do so. It was suggested that the delay line would probably have to be less than ten microseconds total in order to avoid distorting a wave shape with a $\frac{1}{4}$-microsecond rise time and a $\frac{1}{2}$-microsecond width. Further investigation should be made as to how much attenuation will result with various lengths and loadings of the delay line. It was suggested that the delay line could be made with cores (not square hysteresis), so that the output pulses could be transformer-coupled from the delay line. W. Linvill suggested that if square hysteresis cores were used, an improvement would result: If the cores are driven with a step-function instead of a pulse, then the first core would switch and become saturated so that power would then be supplied directly to the next core and cause it to switch (a shunt capacitor being used between each core to provide the necessary isolation between cores before they switch). There was some discussion as to whether this system would work, whether there would be attenuation down the line, and whether the output should be taken from the condenser or from the core by transformer action. W. Papian suggested that a Harvard-type shifting register might be better. Then any amount of power can be taken from any core, and the operation can be stopped on any pulse (by stopping the stepping pulses). It is possible in this application to design the register without using rectifiers. All the registers (one for each instruction) can be shifted on each stepping pulse, because only one core will contain "1". R. Mayer suggested that the control switch merely needs to insert a "1" into the proper stepping channel, so that once this is done, the control switch is not used for the remainder of the instruction. This makes it possible for some other register (or the storage switch) to be used for the control switch at the beginning of each instruction.

The question was raised whether we will be running into the problem of operating cores so fast that they will overheat. It was pointed out that most of the 1 mc activity would be in the arithmetic element and not elsewhere, so that, if the arithmetic element is not made of cores, there will probably be no overheating problems.

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