Digital Computer Laboratory
Massachusetts Institute of Technology
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SUBJECT: PAPER ON FERROMAGNETIC AND FERROELECTRIC MEMORY DEVICES

To: J. W. Forrester

From: W. N. Papian

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Abstract: This paper contains the material for a lecture to be given on September 12, 1952 in the M.I.T. Summer Session course, "Theory and Applications of Dielectric Materials", under the direction of Professor A. R. von Hippel.

INTRODUCTION

In most communications and control systems it is necessary, at times, to "remember", or "store", some of the information which is being processed. This need is particularly obvious in digital computer systems; many pieces of information, such as instructions and numbers, have to be stored away for later use in the computation or control problem at hand.

A number, or "word", is usually stored in a grouping of memory cells called a memory "register". One of the most important problems in digital computer development work today is to develop a very large memory within which arbitrary selection of one out of the many registers is accomplished rapidly and efficiently.

The modern, high-speed, electronic digital computer does its computation in binary arithmetic. As a consequence, the memory cells need store only binary digits; each cell is like a toggle switch which can store a "yes" or a "no", a "ONE" or a "ZERO".

Storage in a Stationary Field

This paper will discuss the storage of binary information in a stationary magnetic or electric field only; moving-part devices (such as rotating magnetic drums) and electromagnetic delay lines will not be introduced.

One type of memory bears early description because it is an introduction to this elementary concept of information storage in a stationary field, and also, because it describes the disadvantages of using linear capacitors or inductors for such storage. The polarity of the charge on a linear capacitor may be defined in terms of binary states, say positive for a "ONE", and negative for a "ZERO". "Reading", or sensing, the information state of the capacitor can then be accomplished either by allowing the voltage across the capacitor to open and close an electronic "gate", or by applying a "write ZERO" voltage pulse to the capacitor and observing whether it reverses its polarity or not (such a reversal would result in an observable pulse of current in the connecting wires). This type of memory has two important practical limitations. One is that the charge does, in time, leak off the capacitor, partly through the dielectric, mostly through the necessary outside circuitry. Secondly, the linear capacitor offers no help in the problem of selecting one out of a multitude of memory cells; some type of selection matrix, containing at least as many non-linear elements (such as crystal diodes) as there are memory cells, becomes necessary.[1] It will be seen later that a good part of the selection mechanism may be "built into" the memory cells in the form of non-linear characteristics, and the loss of information by charge leakage may be avoided by using a material having a high residual, or remanent, charge.

The dual of linear capacitor storage involves storing each binary bit of information in the magnetic field of a linear inductor. Here again selection is difficult and loss of information by the gradual collapse of the magnetic field is even more troublesome.

Three general types of memories now exist which use the flux-remanence and non-linear properties (the hysteresis) of ferromagnetic materials to solve the information-retention problem and the selection problem. They are listed below and will be discussed in the main body of the paper.

1. A parallel-access array with an external selection mechanism.

2. The Harvard stepping register which uses time (or sequence) as its selection coordinate.

3. Multi-coordinate arrays with built-in partial selection.

1. A. W. Holt, "A Very Rapid Access Memory Using Diodes and Capacitors", paper No. 180, delivered at the 1952 National Convention of the I.R.E. in New York. (Mr. Holt is with the National Bureau of Standards, Washington, D.C.)

Basic Memory Property of Hysteretic Device

Illustrated in Figure 1 is a photograph of the 60-cycle flux-current characteristic of a ring-shaped, magnetic-ferrite core which has a "rectangular" hysteresis loop. (The loop may be considered as quasi-static, and, to a rough approximation, it may be taken as the B-H, or flux-density versus magnetic-field-intensity, characteristic). The two points at which the loop intersects the vertical axis are the remanence points, $+\phi_R$ and $-\phi_R$. When the core is at one of these points, the current, I, is zero, and the core acts like a small permanent magnet. For all practical purposes the flux remains at ϕ_R as long as the current remains zero or very small. The two remanence points may be assigned the binary numbers ONE and ZERO; a number may be "written" by applying a large current pulse of the proper polarity and duration; the number will be "stored" for an indefinite period of time and can be "read" by observing $d\phi/dt$, the e.m.f. produced across a winding on the core, during the application of another current pulse. The core, when used in this manner, may be classed as a bi-remanent memory device. Note that the flux-remanence property of the core makes it possible to maintain a flux magnitude and polarity with zero applied current or magnetizing force. Loss of information by the collapse of the magnetic field at zero magnetizing force, as it occurs for the linear inductor, is thus avoided.

The charge remanence property of a ferroelectric capacitor may be used to avoid the analogous loss of information due to the collapse of electric field in a capacitor memory device. The charge-voltage characteristic of such a capacitor should resemble Figure 1 with the letter substitutions of Q for ϕ and V for I. The stored charge remains at Q_R even though the capacitor is short-circuited and the voltage reduced to zero.

The extreme non-linearity of the hysteresis loop is also an aid in the selection problem. Any memory element which is insensitive to an applied field of a given magnitude but does respond to twice or three times that magnitude can be operated, along with many others, in a large matrix or array wherein element selection is accomplished at the junction of two or three physical coordinates. This is the third type of memory in the list of included devices; its solution of the onerous selection problem is very neat and promising.

SOME MEMORY SYSTEMS

Single-Coordinate Register Selection, Parallel Access Array

Where the digits of a stored word are wanted in parallel, that is simultaneously, and the memory is not too large, it is practicable to use linear, or single-coordinate, register selection. The principle of such a system is illustrated schematically in Figure 2. The rings represent small ferromagnetic cores whose hysteresis loops exhibit "rectangularity" *along with* high flux remanence. Register selection in this small (2-register, 2-digit) memory is accomplished by the single-pole, two-position switch; circuit connections are made by it to the desired register. During the "read" operation, the circuit looks effectively like Figure 2a. "Read" current is supplied through the selection switch to all of the cores in the desired register and the resultant induced voltage is fed out on to the digit busses. The register is left full of ZERO's, or "cleared", and ready for a "write" operation. The effective schematic during the "write" operation is illustrated in Figure 2b. Here, "write" currents are supplied only by those digit busses which hold a ONE. These currents sum and are returned through a selection switch. Non-linear elements in the form of diode rectifiers act as isolators to prevent "sneak" currents from taking their complex paths through the array.

The flux-remanence aspect of the hysteresis loops of the cores allows information retention at zero driving currents, but no attempt is made to use core characteristics to aid in the selection problem. This type of memory uses at least one diode per stored "bit" plus a single-pole, n-position, electronic selection switch, where n is equal to the desired number of registers. The number of diodes and the size and current-capacity of the switch become prohibitive as the size of the memory is increased above a few hundred registers.

Time or Sequence Selection

The Computation Laboratory of Harvard University has done a large amount of pioneering work in the application of magnetic cores to digital computer problems. Their principal contribution was the development of a device they called the Static Magnetic Delay Line[2].

2. An Wang and Way Dong Woo, "Static Magnetic Storage and Delay Line", Journal of Applied Physics, 21, 1, (January, 1950)

It might also be called a shifting register or stepping register, and it consists of a line of cascaded memory cores so arranged that information can be shifted or stepped down the line sequentially, at a rate determined by a primary pulse source, until the information comes out at the end. As it is now being used at Harvard, the line requires two cores and four diode rectifiers per stored binary digit.

The line is basically a serial memory device; parallel access to a word may be accomplished by using a group of lines, one line for each digit of the stored word. Words can then be stored and read only in time sequence, so that the coordinate for register selection may be said to be time or sequence.

Cores with high flux remanence are used, again to avoid information loss due to field collapse, but no attempt is made to use the core's non-linearity to carry part of the selection burden.

The Static Magnetic Delay Line makes a fine memory of the serial type; it also makes a fine buffer memory between computer elements which run at different speeds. It is not, however, a strong candidate for the large, high-speed, parallel, arbitrary-access, internal memory job.

Multi-Coordinate Register Selection

Register selection may be accomplished at the junction of two or more physical coordinates. Ferromagnetic and ferroelectric memories of this type are being developed at M.I.T.[3], at R.C.A. Laboratories,[4] at Bell Telephone Laboratories[5], and possibly elsewhere. This application puts more stringent requirements on the cores than do most applications. The memory system will be described in some detail and the material requirements derived accordingly.

3. Forrester, J. W., "Digital Information Storage in Three Dimensions Using Magnetic Cores", Journal of Applied Physics, XXII (January 1951)

4. Rajchman, Jan A., "Static Magnetic Matrix Memory and Switching Circuits", RCA Review, XIII, 2 (June 1952)

5. Anderson, J. R., "Ferroelectric Materials as Storage Elements for Digital Computers and Switching Systems", Conference paper delivered at the Winter General Meeting of the A.I.E.E. in N.Y.C. on January 24, 1952.

Figure 3 shows one of the internal hysteresis (ϕ vs I) loops of the magnetic-ferrite core used in a successful memory array. The selection scheme in this array depends on the fact that a current of magnitude I_m can change the flux in a core from $-\phi_R$ to $+\phi_R$, whereas half that current ($I_{m/2}$) has a neglible effect. This is a consequence of the high degree of non-linearity shown by the sharpness of the "knees" of the loop.

If, for example, nine such cores are arranged in a planar array, as in Figure 4, and currents $I_{m/2}$ are caused to flow coincidentally in selected lines x_3 and y_2 as shown, core F is the only core in the array which has the full magnetizing force (I_m) impressed. The others have either half or zero magnetizing force impressed. Each core is, in this arrangement, a coincidence device, and the only core whose flux is significantly affected is the one at the junction of the selected lines. (The output voltages may be taken from the sensing windings, S, after suitable mixing).

The extension to three dimensions may be accomplished by stacking these two-dimensional arrays along a z axis, with corresponding x lines connected in common and corresponding y lines connected in common. In this arrangement the application of $I_{m/2}$ to an x line and a y line results in the selection of a line of cores parallel to the z axis, that is, a register. To "write ZERO" in some of the cores of the selected register it is only necessary to "inhibit" those z planes by applying to them an opposing polarity current of half magnitude.

Variations on the selection scheme described above have been devised which impose slightly less stringent requirements on the core. It is possible for the core to have to discriminate between currents which bear 3:1, 5:1, or greater ratios to each other[6]; advantage may be taken of these greater current ratios to reduce switching times, increase signal-to-noise ratios, or relax some of the hysteresis-loop requirements. The cost is an additional increase in the electronic equipment surrounding the system for each increase in the current ratio.

Figure 5 is a photograph of a planar ferrite memory array now operating at M.I.T. The 256 small memory cores occupy the square in the

6. Everett, R. R., "Selection Systems for Magnetic Core Storage", Engineering Note E-413, August 7, 1951, an internal document of the Digital Computer Laboratory, M.I.T.

center of the picture. The x and y driving windings consist merely of the wire grid upon which the cores are mounted. A closeup view in Figure 6 shows this somewhat better; size may be judged from the heavy coordinate wires, which are A.W.G. no. 20 enamelled magnet wire.

The dual of this type of memory is not difficult to visualize. One possible arrangement is illustrated in Figure 7. The voltages shown are for a selection scheme which gives 3:1 voltage ratios. The barium titanate slabs available at M.I.T. have not had sufficiently rectangular Q-V loops to operate as coincident-voltage memory cells at 2:1 voltage ratios; results have been better but not yet good enough with 3:1 ratios. The barium titanate slab containing the experimental 8-by-8 memory may be seen at the top of Figure 8. In the upper compartment of the "cage" may be seen a ferritic core "current transformer" which is used in the sensing circuitry.

MATERIALS EVALUATION AND TESTING

In order to judge between various ferromagnetic and ferroelectric materials, it becomes necessary to set up relevant criteria to describe, as quantitatively as possible, the ability of the parts of the memory system to process information accurately and rapidly. The ONE-to-ZERO output-signal ratio and the switching (or flux-reversing) time tell a great deal about a simple magnetic-core memory unit of the non-coincident-current type. Criteria for the coincident-current unit are somewhat more involved, and will be discussed in some detail.

Information Retention and Loop Shapes

Refer to Figure 9 and let an "undisturbed ONE" be defined as the $-\phi_R$ flux state of the core and an "undisturbed ZERO" as the $+\phi_R$ state. Let a "read" pulse of current be arbitrarily fixed at $+I_m$ so that reading a ONE results in a large flux change and a correspondingly large output pulse, and reading a ZERO gives a small output pulse. A ZERO is, then, "written" by a $+I_m$ pulse also, and a ONE is written by a $-I_m$ pulse.

Recall that selecting one core in a two-or-three-dimensional array results in the application of $I_{m/2}$, called a "nonselecting" pulse, to cores elsewhere in the array. The application of repeated nonselecting read pulses to a core containing a ONE tends to run the state

of that core up along the ϕ axis, as indicated by the dashed lines in Figure 9, disturbing or destroying its information. When the hysteresis loop is properly rectangular and all parameters correctly adjusted, the operating point moves up the axis only to some asymptotic position not far above the point $-\phi_R$, and the core operates satisfactorily in the coincident-current scheme.

A core which contained an undisturbed ONE and has been subjected to a large number of nonselecting read pulses is considered to hold a "disturbed ONE". By the above reasoning, the disturbed-ONE output is usually lower than the undisturbed-ONE output.

In an analogous manner, repeated nonselecting write-ONE pulses will run the core's operating point from $+\phi_R$ downward, increasing the size of a ZERO output pulse so that a disturbed-ZERO output is usually larger than an undisturbed-ZERO output.

Since nonselecting disturbances may reduce the output signal from a core containing a ONE and increase the output from a core containing a ZERO, the ratio of the disturbed-ONE output to the disturbed-ZERO output, called the "disturbed-signal ratio", is a critical measure of a core's performance as a coincident-current memory unit. This ratio approaches infinity in the ideal case, and should be much greater than one if reasonable discrimination between the binary digits is to be obtained.

The application of a nonselecting pulse to a core results in a voltage output, or form of noise, called a "nonselecting output". The ratio of a disturbed-ONE output to a nonselecting output, called the "nonselecting signal ratio", is another important criterion of operation. Like the disturbed-signal ratio, it approaches infinity in the ideal case and should be much greater than 1 for satisfactory operation.

The two ratios mentioned above are functions, largely, of the shape of a core's ϕ-I loop. The values of the ratios approach the indicated ideals as the rectangularity of the hysteresis loop increases.

From the idealized hysteresis loop of Figure 9A, some necessary conditions for coincident-current operation may be stated. A loop must exist for which the following relations hold true:

$$I_M > I_2$$

$$\frac{I_M}{2} < I_1$$

where I_1 and I_2 are the points at which the ϕ-I curve changes direction abruptly. Combining these gives one general requirement on the hysteresis loop shape,

$$I_2 < 2I_1$$

Experimental results give qualitative support to this general requirement.

Pulse Testing

Previous considerations lead directly to the magnetizing pulse patterns desired for signal testing. Two of these patterns are illustrated in Figure 10; mode a consists of alternate-polarity, full-amplitude pulses for checking an undisturbed-ONE; mode b checks a disturbed-ONE by interspersing a large number of half-amplitude nonselecting pulses between the negative (write-ONE) pulse and the positive (read) pulse. The response to the nonselecting pulses may also be observed during mode b operation. Other modes check for undisturbed and disturbed ZEROs. (Pulse amplitudes, lengths, spacing, and the number of intervening nonselecting pulses are independently variable).

Core ϕ-I characteristics were generally observed at low frequencies by the usual methods.

Response times were taken to be the lengths of the disturbed-ONE output pulses, and the length of the test pulses was kept somewhat larger than this.

Many cores were tested. The problem was well illustrated over a year ago by two of them, one metallic, the other a magnetic ferrite. The metallic core, made by Allegheny Ludlum of one-mil "Silectron" tape, had excellent signal ratios; its response time, during the reading of a ONE, was about 25 microseconds. Scope traces for this core, for the disturbed-ONE mode and the disturbed-ZERO mode, are shown in Figure 11; arrows point to the pertinent output pulses. The disturbed-signal ratio and the nonselecting signal ratio are both obtainable from these traces. (The time scale is 5 microseconds per large division.) The negative trace in the upper photograph is the core output when the ONE is written; the heavy center trace combines the large number of nonselecting outputs which follow the writing; and the final disturbed-ONE output shows as the large positive pulse. The positive trace in the lower photograph is the output from the read or write-ZERO operation; the interspersed nonselecting write-ONE pulses merge in the heavy negative trace.

A very promising material for high-speed work in this field is magnetic ferrite. Good results were obtained with a General Ceramics and Steatite core, which had fair signal ratios and a response time near one-half microsecond. Figure 12 shows scope photographs for this core under two conditions. The first column was taken for I_M adjusted to optimum amplitude. The second column was taken with too large an I_M amplitude, resulting in an increased disturbed-ZERO output and a decreased disturbed-ONE output. This led to an unsatisfactory disturbed-signal ratio close to one in value.

The table in Figure 13 summarizes the important test results for the two cores and compares them with today's cores and the ideal values shown in the last column. (The signal ratios are taken from the voltage-time areas of the output pulses; this gives a rather pessimistic, but fundamental, measure of a core's characteristics.) Note that the major improvements have come to the metallic cores as a reduction in response times and to the ferrites as increases in signal ratios. The data for the 1952 metallic core were taken on a 79-4 Molybdenum Permalloy core wound of 1/8-mil ribbon by Magnetics, Inc.; the ceramic core is of Ferramic 1118.

One other important core characteristic is the amount of single-turn driving current it requires (I_M) when operating as a coincident-current unit. This is dependent on the size of the core and its coercivity. These current values are roughly 0.3 ampere and 3.0 amperes respectively for the metallic and ceramic cores now operating at M.I.T.

Development Program

The improvement of ferromagnetic and ferroelectric materials for use in computer circuits is being carried on at two levels. A large amount of empirical development work is being carried on by commercial manufacturers. A fundamental investigation of ferrites is being undertaken at M.I.T. by the Laboratory for Insulation Research and the Digital Computer Laboratory. This program is aimed at a better understanding of the basic nature of the ferrites so that characteristics can be improved and controlled during synthesis. The goal is to be able to specify an explicit synthesis procedure for a material having certain characteristics determined by the intended application. New applications for ferromagnetic and ferroelectric materials in digital computers may call for other characteristics; these will be studied as the applications become more definite.

CONCLUSION

Storage of binary information in the stationary field of a ferromagnetic ring or a ferroelectric slab promises a neat solution to one of the most vexing problems in the digital computer field, the problem of "remembering" and making available a very large number of binary "words" rapidly and efficiently. The flux-remanence and non-linear characteristics of the "rectangular" hysteresis loop simplify the information-retention and the word-selection aspects of the problem tremendously.

Highly rectangular hysteresis loops, high speeds, low losses, low driving requirements, excellent quality and uniformity, and reasonable cost are among the characteristics desired in these materials for the applications in view. Freedom from aging and deterioration are also extremely important.

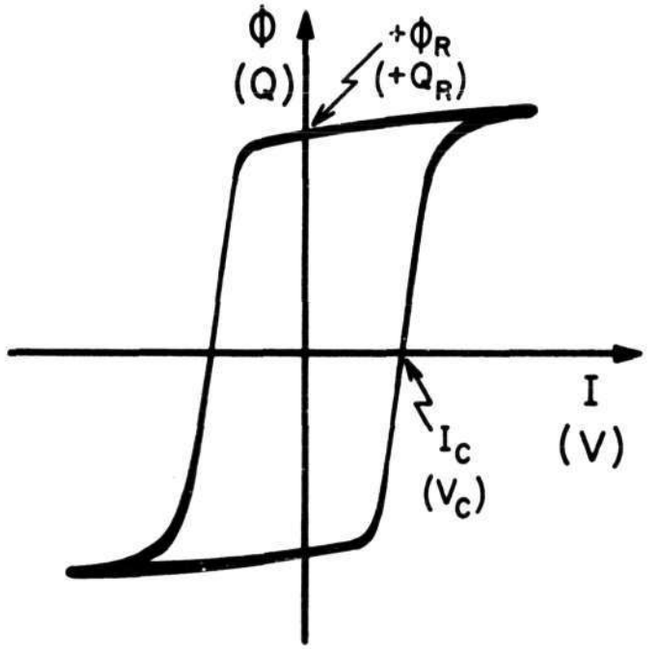
Material improvements during the last two years have been encouraging, and much future progress is expected.

Signed William N. Papian
W. N. Papian

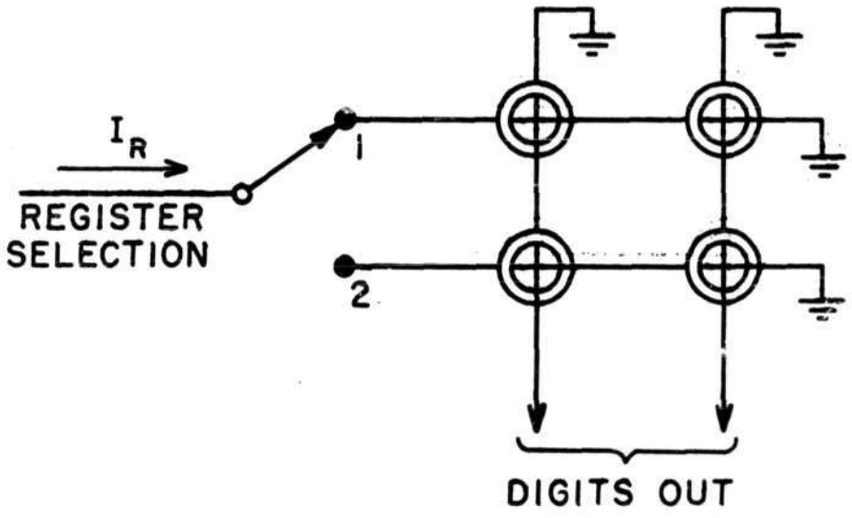
WNP:jmm

Approved N. H. Taylor
N. H. Taylor

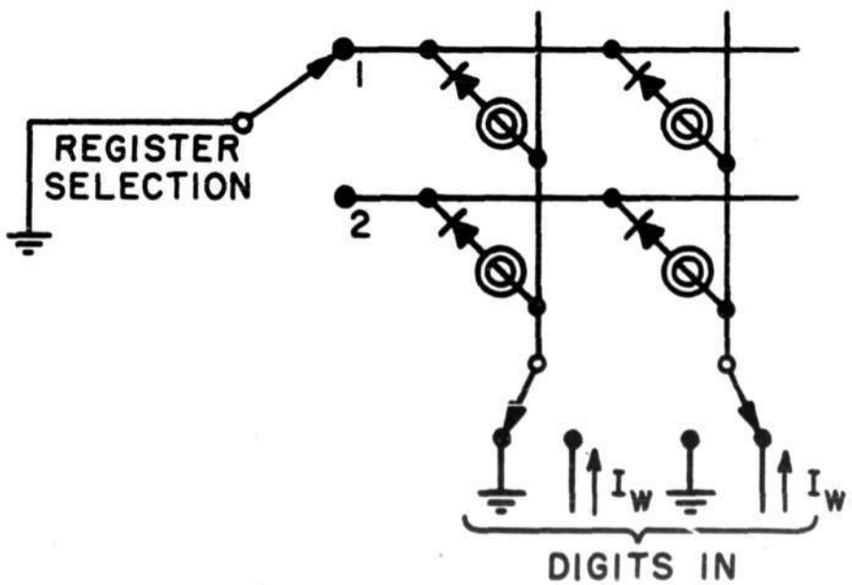
List of Illustrations



HYSTERESIS LOOP
(FERRAMIC 1118-259)



(a) READ

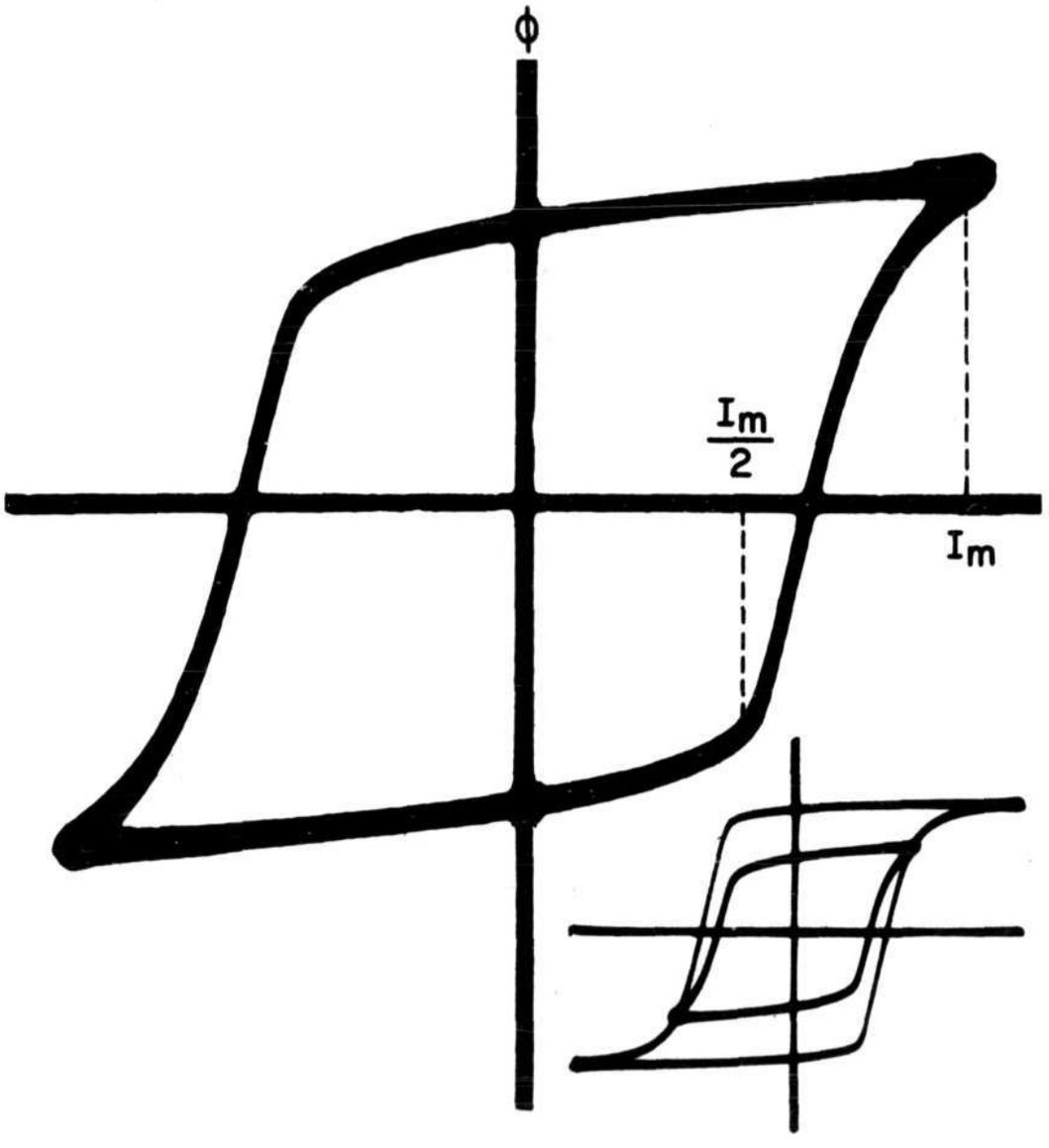


(b) WRITE

FIG. 2 SINGLE-COORDINATE REGISTER SELECTION

A-52000

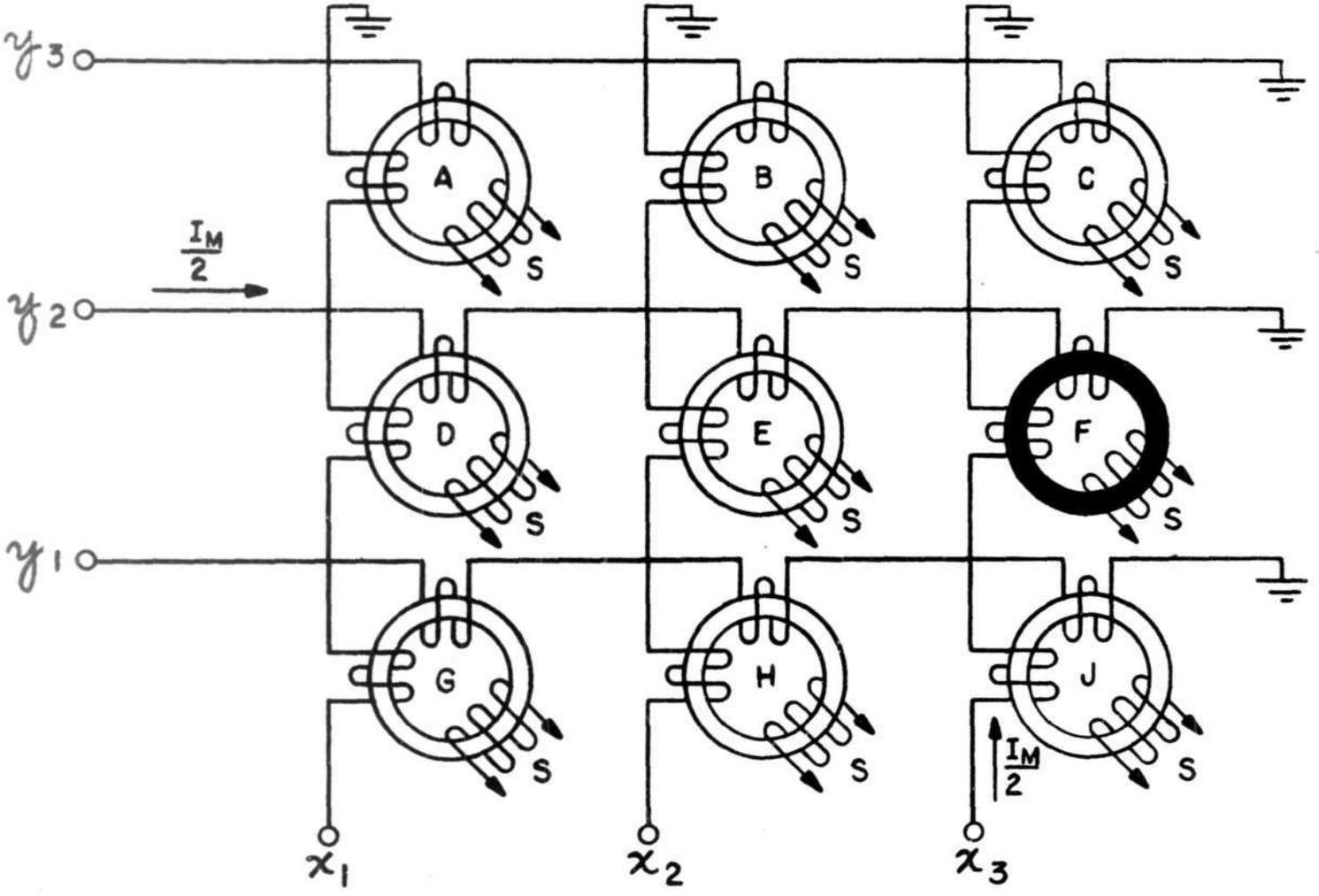
FIG. 2



ϕ-I LOOP FERRAMIC 1118 (259)

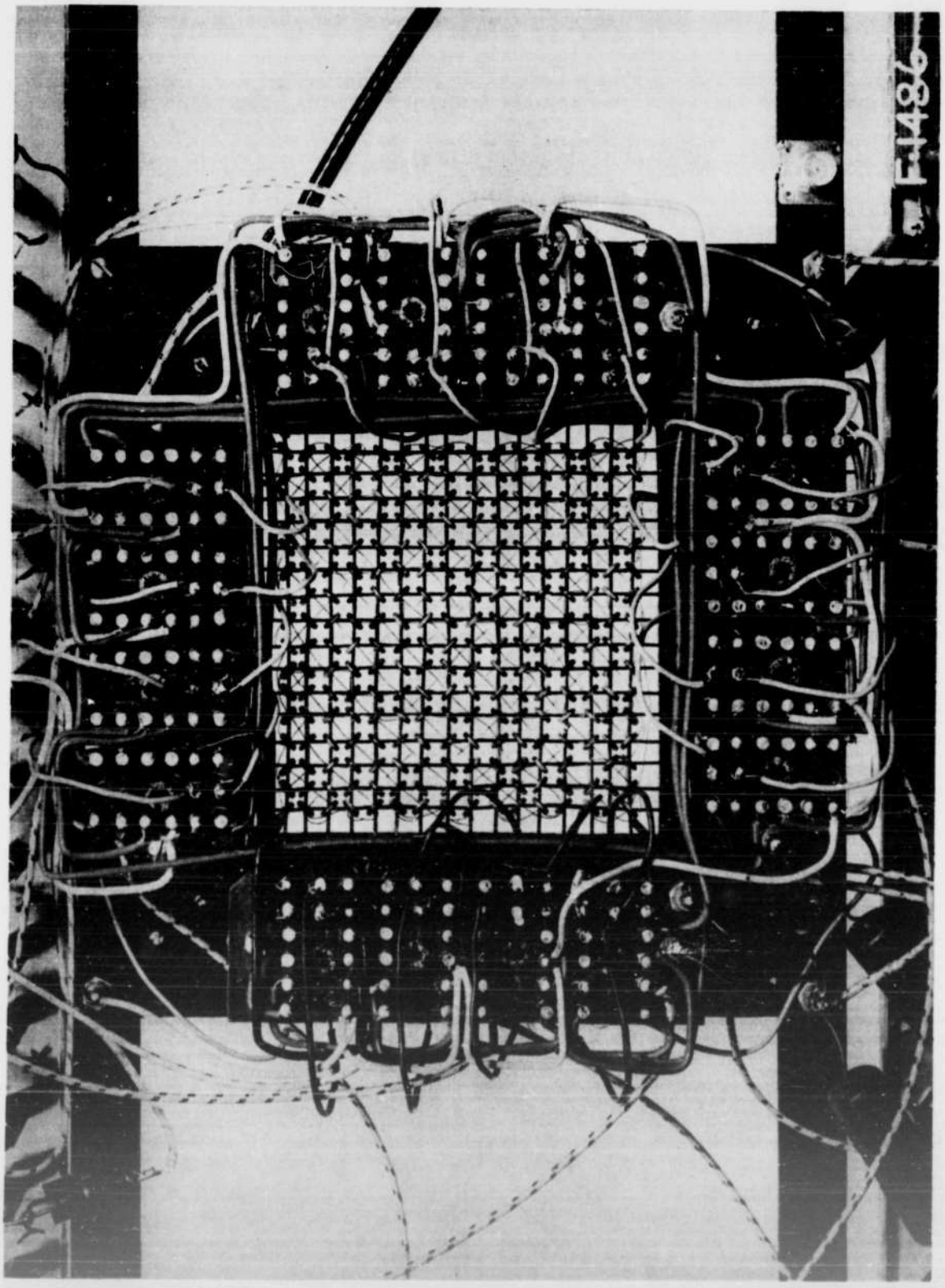
A-51527

FIG. 3



A TWO-DIMENSIONAL ARRAY OF CORES

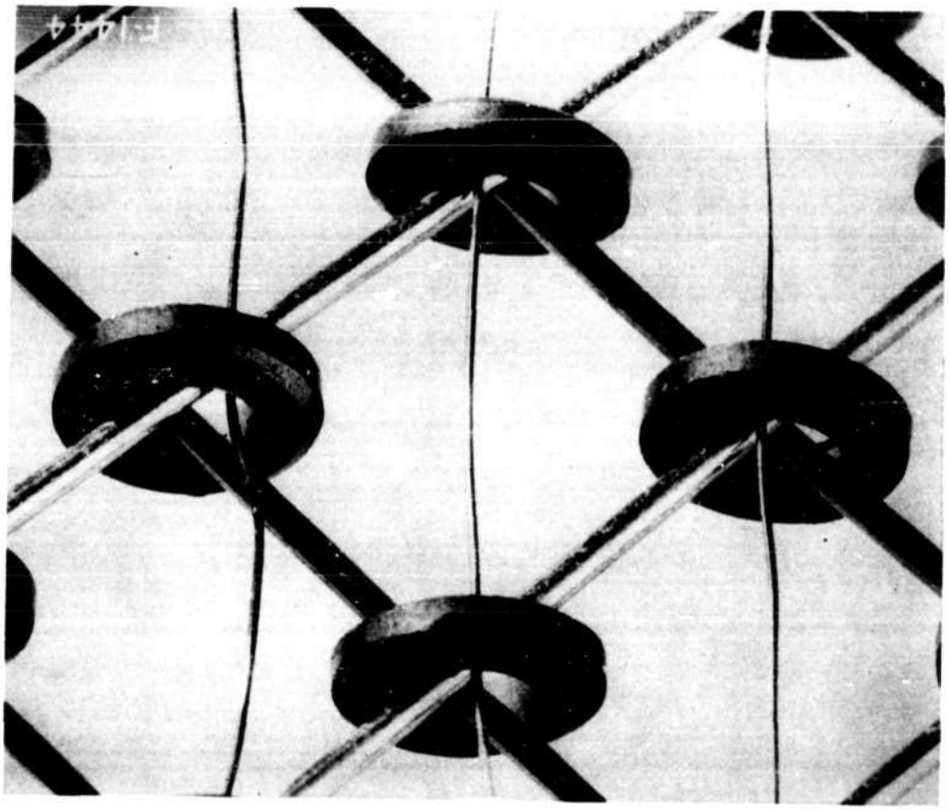
FIG. 4



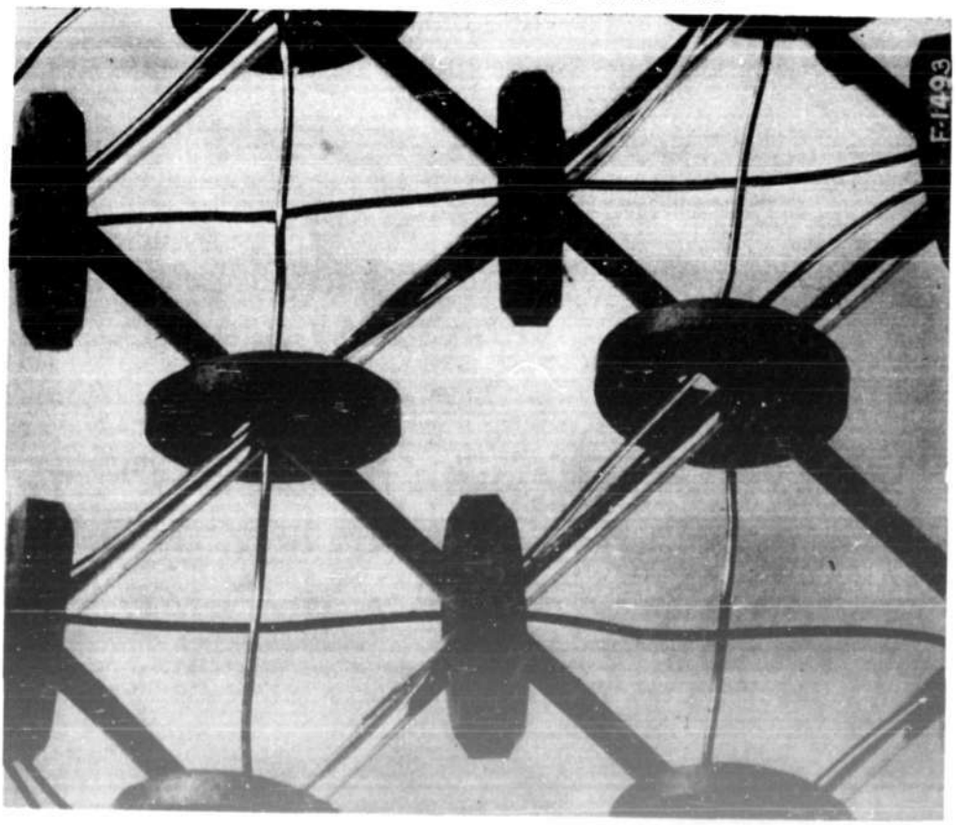
CLOSE-UP OF CERAMIC MEMORY I

A-51447

FIG. 5



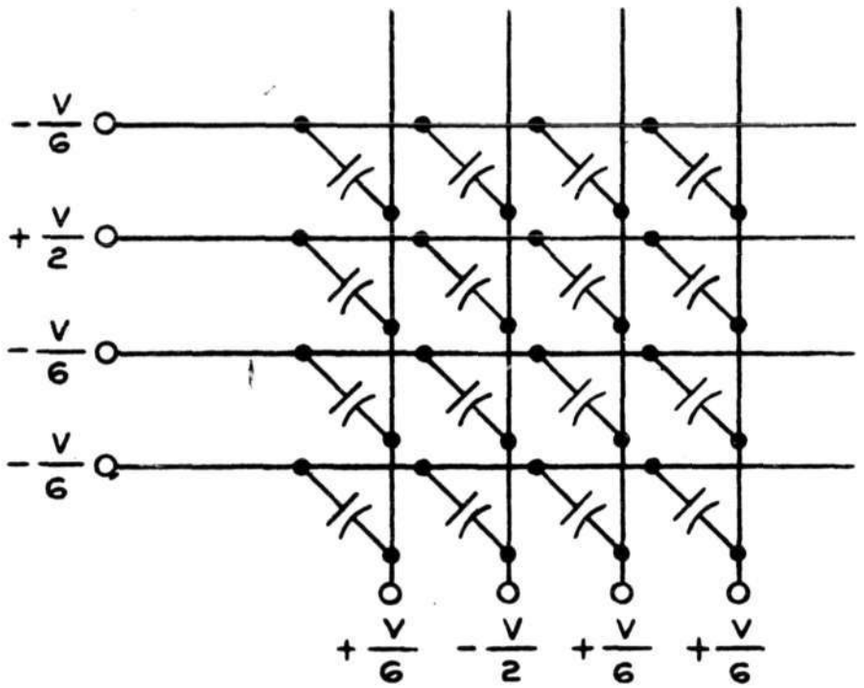
MEMORY WITHOUT Z WINDING

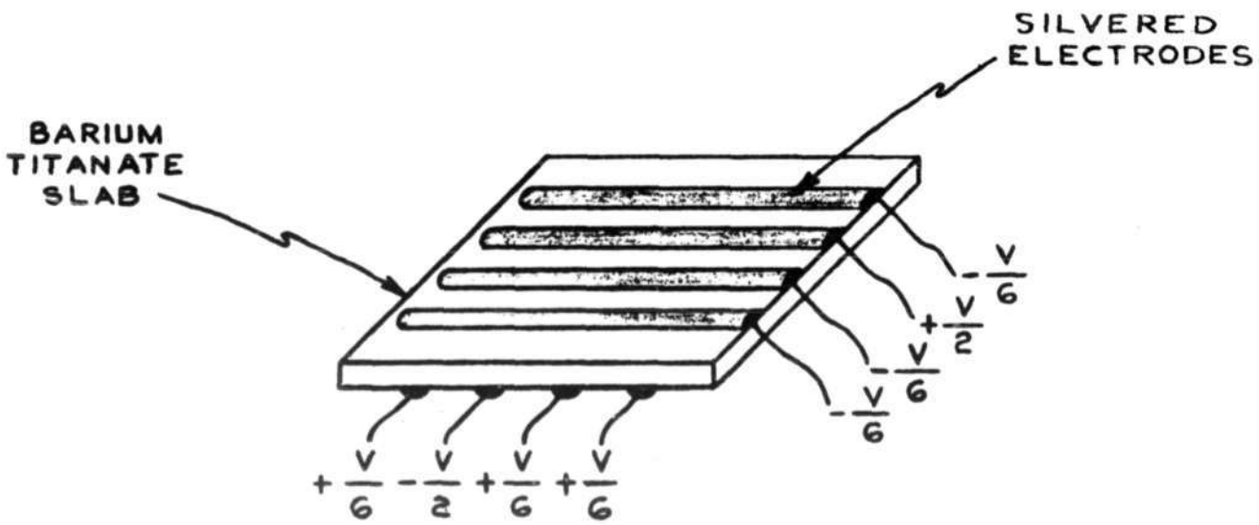


A-5465
F-1493
F-1914

MEMORY WITH Z WINDING

FIG. 6

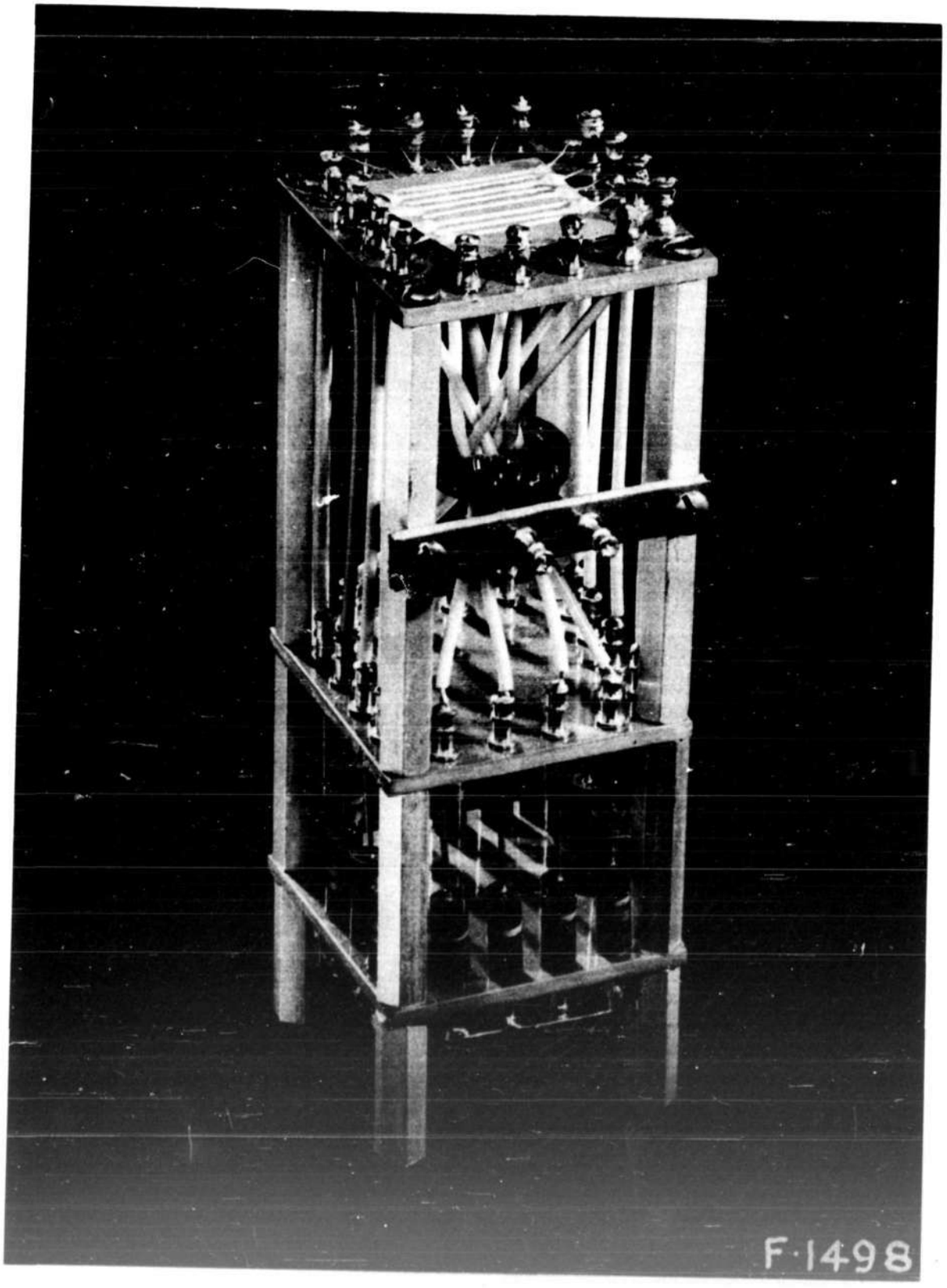




FERROELECTRIC MEMORY

A-50550
MN

FIG. 7



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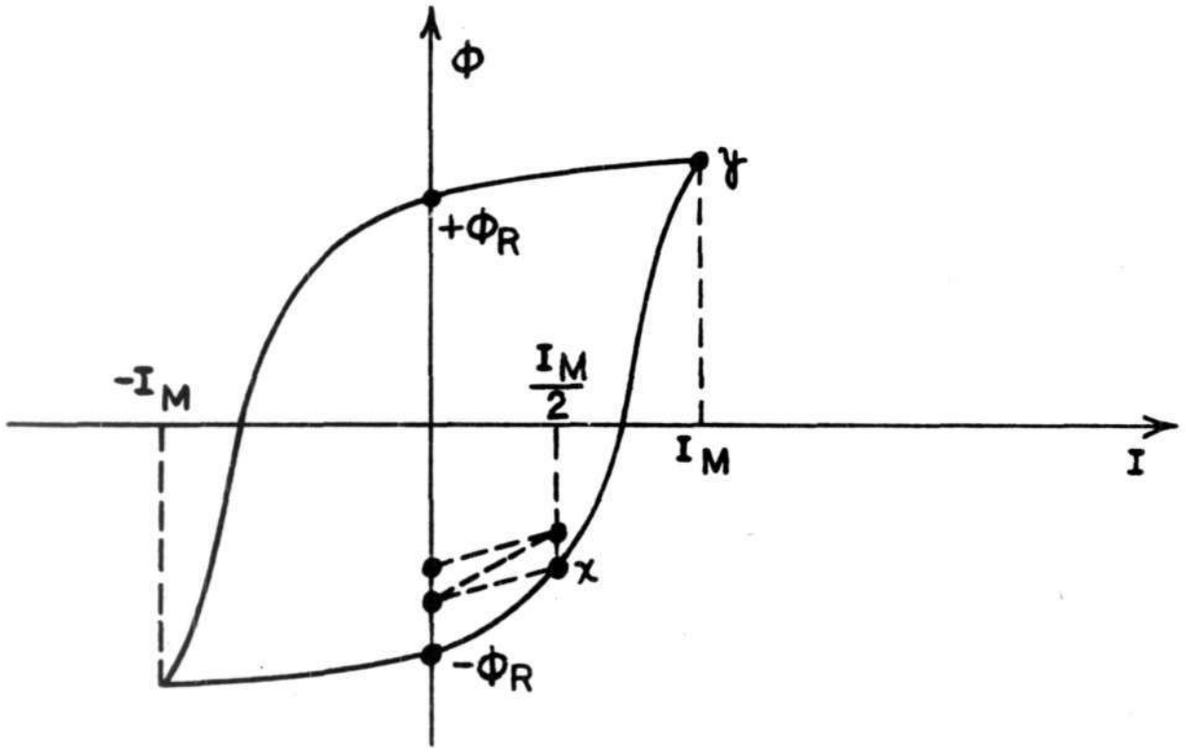
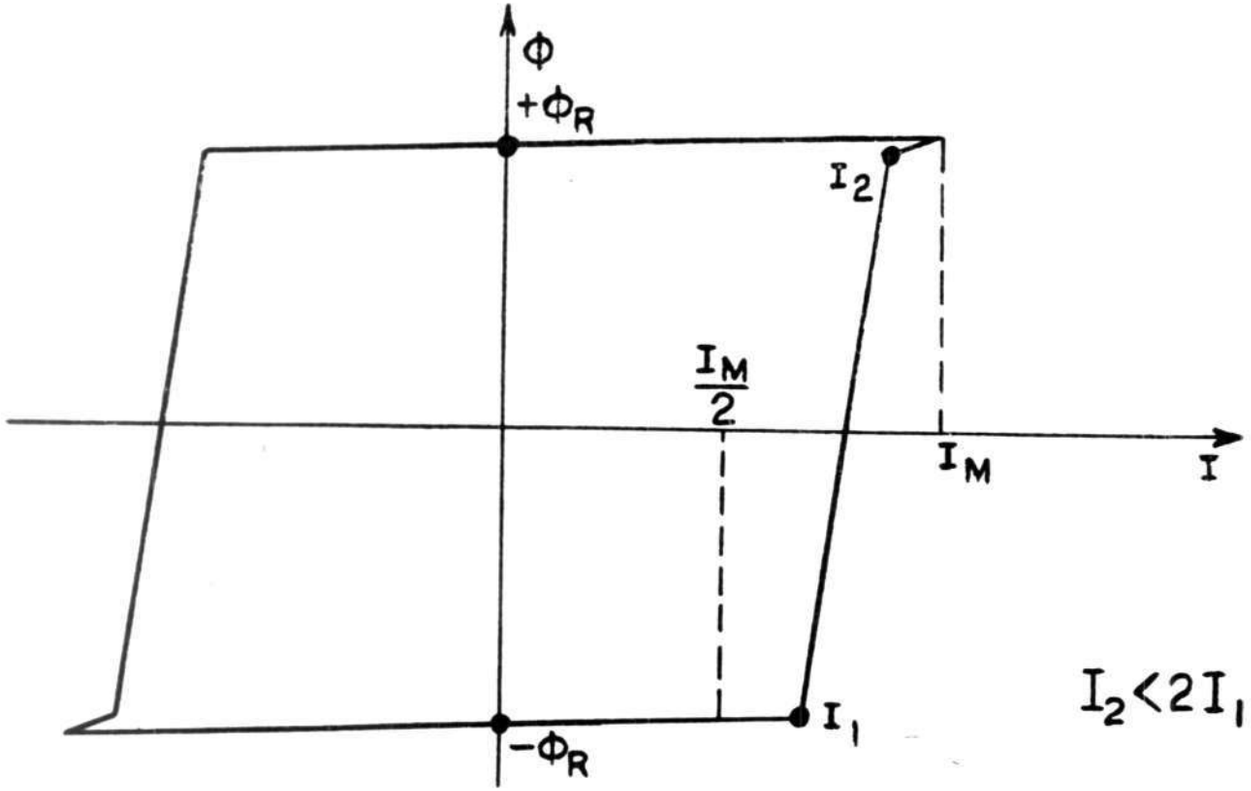
EIGHT BY EIGHT FERROELECTRIC MEMORY

FIG. 8



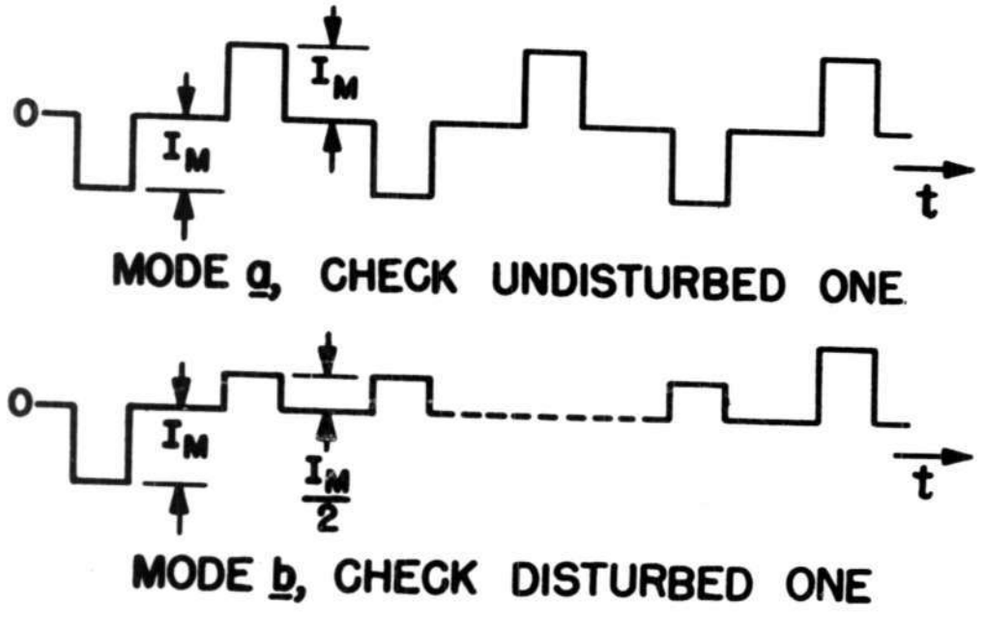
PATHS OF OPERATION OF A MAGNETIC MEMORY UNIT

FIG. 9



AN IDEALIZATION OF A Φ−I LOOP

FIG. 9A

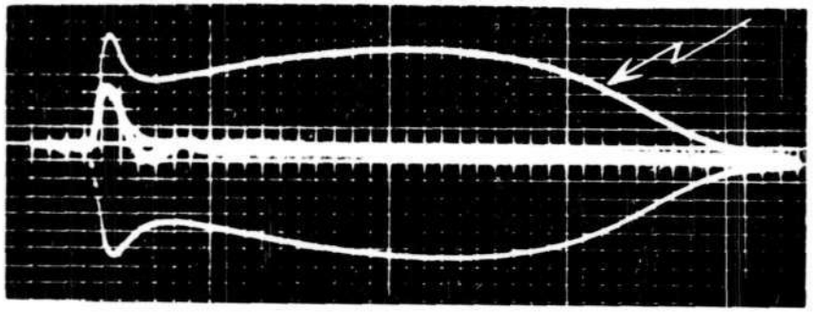


CORE-TESTING PULSE PATTERNS OF I

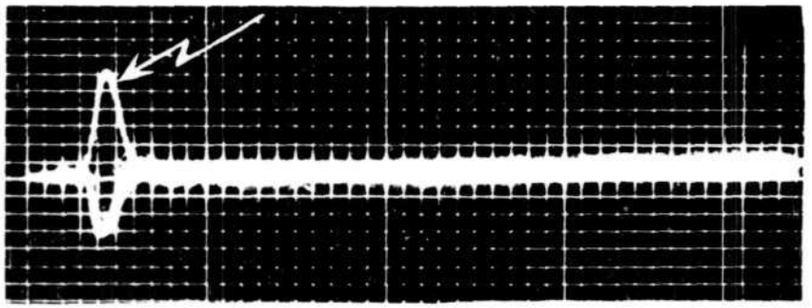
FIG. 10

A-36615-1
F-1266

DISTURBED ONE

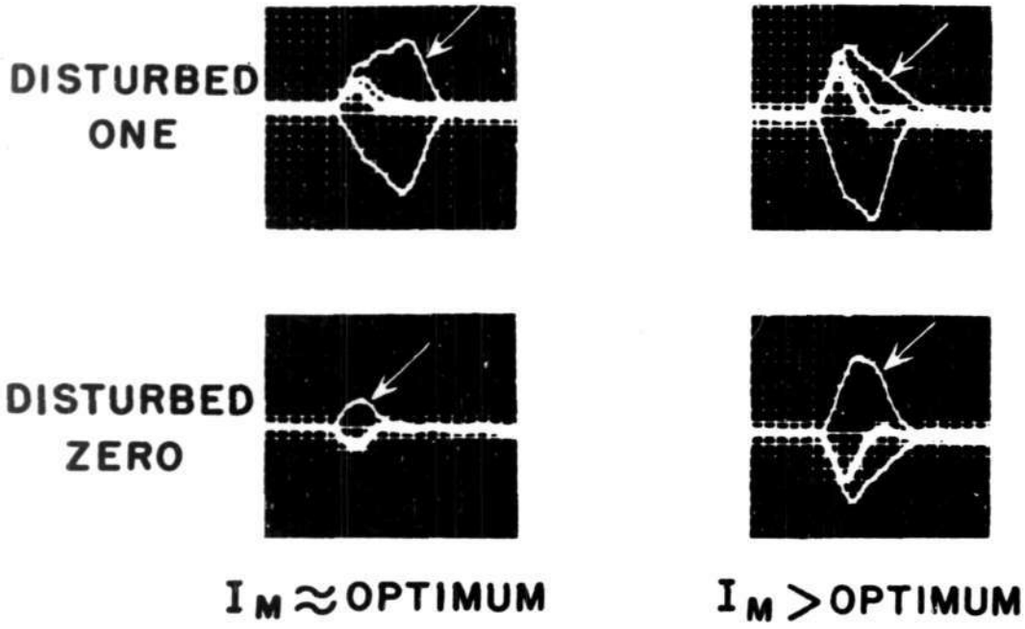


DISTURBED ZERO



COINCIDENT-CURRENT TEST RESULTS, BEST METALLIC CORE (1950)

FIG. 11



COINCIDENT-CURRENT TEST RESULTS,
BEST FERRITIC CORE
(1950)

FIG. 12

CORE CRITERIA	BEST METALLIC		BEST FERRITIC		IDEAL
	1950	1952	1950	1952	
DISTURBED-SIGNAL RATIO	13	18	6	10	$\rightarrow \infty$
NON-SELECTING SIGNAL RATIO	16	20	3	10	$\rightarrow \infty$
RESPONSE TIME (μ SEC)	25	10	$\frac{1}{2}$	$\frac{3}{4}$	$\rightarrow 0$

CORE COMPARISONS

FIG. 13