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Auth: DD 254 Digital Computer Laboratory
By: R.R. Everett Massachusetts Institute of Technology
Date: 12/2/59 Cambridge 39, Massachusetts

SUBJECT: Second Meeting on Air Defense Computer, Nov. 6, 1951

To: Jay W. Forrester

From: B. E. Morriss

Date: November 7, 1951

Present were:

- Forrester, Jay W.
- Adams, C. W.
- Brown, D. R.
- Everett, R. R.
- Israel, D. R.
- Morriss, B. E.
- Papian, W. N.
- Taylor, N. H.
- Walquist, R. L.

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The meeting opened with several statements or questions by R. L. Walquist. The question of dual or multiple storage systems versus a single storage system was raised. While the multiple selection system would necessarily contain more equipment than a single system, the additional amount is dependent upon the natural breakdown due to the particular type of storage and the manner in which it is used. No attempt was made to determine this amount. It was stated that with multiple storage systems the individual selection systems would be utilized a much smaller percentage of the time than with a single selection system, but this would be partly offset by increased operating time for the arithmetic element.

The question of selection of stored information in steps was brought up again. The idea was to select and remove a block of information from storage in one operation and then to select and remove single words from this block later. While this might speed up operations in a slow-access storage system, the objective here was to reduce the amount of switching equipment necessary. It was suggested that Walquist and Israel work on this and discuss it with Adams and Taylor before presenting

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the results to the group. Later in the afternoon this was discussed in more detail. With respect to magnetic cores, no simple method of reading out blocks was found which did not utilize more equipment than the complete selection methods originally proposed for two- or three-dimensional arrays.

N. H. Taylor said that the speed visualized for Whirlwind II was 10-20 μ s for an average order including storage access, or 6-12 μ s without storage access. Multiplication times could be of the order of 2 μ s per digit. It was mentioned that there were no logical reasons why the storage accesses had to occur at times different from those in which the operations were actually being carried out. The partial overlap of program timing and operation timing as found in Whirlwind I may be extended so that both the order and the word on which to operate are removed from storage while the previous order is being carried out. This would effectively reduce the time per order by the amount of time necessary to perform the faster of these two operations (reading from storage and carrying out the order) and only in the case of sp's and cp's which take effect would the reading of the contents of the address register have been done in vain.

D. R. Israel brought up the question of necessary reliability and attempted to extrapolate the expected time between failures from the predicted failure rates of components. It was pointed out that this did not necessarily follow because there was no obvious correlation between the failure of components and errors. Components have been removed whenever anything peculiar is observed. (Example: slight jitter or drift in a crystal.) Thus it is impossible to determine if component has ever caused an error, or even if it might cause an error in the future due to the reason it was removed. Three-quarters of the crystals removed from Whirlwind I have been caught in this manner and while some have probably caused several random errors, many may not have caused any errors. A sharp distinction must be made between the types of errors permissible and checking and correcting methods for computers performing computational problems when the problem can be easily stopped and the trouble found and fixed, and a computer operating on a real-time problem where a continuous output is necessary. Necessary reliability against different types of errors is certainly a function of the time necessary to locate and correct the trouble causing these errors.

N. H. Taylor began an explanation of a magnetic core counter but was forced to leave before the explanation was completed. This will be completed at a later date. He expressed the opinion that it was desirable to develop some feeling for the basic blocks which could be

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formed from cores, and it was suggested that someone from the group working on magnetic cores should discuss possible ways of building counters, adders, etc. from cores.

A brief discussion was held on the possible operating temperatures of magnetic cores. W. N. Papian expressed the belief that the possible operating range was quite large. While they were not proof of retention of rectangularity of hysteresis loops, permeability vs. temperature charts were presented. This question appeared to be quite important since it would determine the best dissipation possible. The problem of heat dissipation is important in determining the duty factor possible for the cores. This has been one of the limiting factors of the present stepping registers which must dissipate about 5 watts at 100 kc. Mr. Papian said he would have experiments run on the cores at different temperatures and report the results.

Mr. Everett then discussed some ideas he had worked on for a simplified computer (See Figure 1). Basically the ideas were the use of a single register to modify information and specific storage registers to hold the information normally stored in flip-flop registers. The register which serves as the input to storage and receives the output of storage was called the Electronic Register, ER, because it is the only register other than the storage selection register, SR, and the control switch register which is similar to present registers. Except for its ability to shift and add it is similar to the present program register. When it is necessary to modify the contents of one of the registers such as PC or AC, it is read into ER, modified, and returned to storage. Thus in proceeding from one order to the next, the storage register which serves as PC would be read into ER, one would be added to ER, and the contents of ER read back into storage and into the storage selection register.

Except for limitations of speed, the ideas presented by Everett do not require any definite type of storage or storage selection. Because magnetic cores in a two-dimensional selection pattern seem to work well in conjunction with this scheme, the examples used assume such a storage system with the selection system making use of the Olsen magnetic gating effect. Since this gating effect requires a write after every read to reset the switch those writes which are not required in the actual execution of the order are marked by an asterisk*.

Little was said about the control necessary other than it was hoped that this could also be formed largely of magnetic cores and probably should consist of a variable length time pulse distributor. It would be

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simplified by the large reduction in number of places to which pulses are sent, if for no other reason. Mr. Walquist raised the question of using storage to hold parts of control as well as arithmetic element and other registers. The storage selection register is used for some control functions. It is made as a counter and used to count shifting pulses and to move storage selection in cyclic patterns as will be seen in the multiply order.

add

The clear and order, ca, will be explained in some detail followed by a listing of operations for ts, cp, and mr. Storage registers are cleared by reading out and rewriting must take place if the contents are not to be destroyed. It is assumed that a convenient method exists of reading into and out of a few specified storage registers such as that containing the accumulator without disturbing the storage selection register. If this is not so, then slightly more operations will be needed. Storage register 0-0 will be considered the program counter, register 0-1 the accumulator, and 0-2 and 0-5 to 0-15 temporary storage registers.

Clear and Add - ca

1. Read Out 0-0 to ER (PC)
2. Add one to ER
3. Rewrite in 0-0 (PC)
4. Transfer contents of ER to SR
5. Clear ER and read out of selected register
6. Rewrite in selected register

Transfer order section of ER to control switch, storage address section to SR

8. Clear ER and Read out of selected register to ER
9. Rewrite
10. Read 0-1, but inhibit reading into ER (clears AC)
11. Write contents of ER in 0-1 (AC)

Steps 1 to 4 perform the task of determining the register containing the next order in the sequence and setting up the storage selection switch to obtain this order and address. Steps 5-7 obtain the order and address and set the control switch to perform the order and the storage selection switch to select the proper address. Thus

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steps 1-7 perform the program timing. Steps 8 and 9 obtain the word to be placed in AC. Order 10 clears AC by reading it out, but not into ER since it is not to be added to the number in ER. This is the only difference between ca and ad. Order 11 then transfers the word in ER into storage register 0-1 which represents the accumulator. The computer is now ready to perform the next order by clearing the storage selection switch and beginning with step one again.

Transfer to Storage - ts

1. Read out 0-0 (PC) to ER
2. Add one to ER
3. Rewrite in 0-0 (PC)
4. Transfer contents of ER to SR
5. Clear ER and read out of selected register
6. Rewrite in selected register
7. Transfer order section of ER to control switch, storage address section to SR
8. Read out 0-1 (AC) to ER
9. Rewrite
10. Read out selected register but inhibit read in to ER
11. Write in selected register.

cp

Operation timing shown below preceded by program timing.

8. Read out 0-2 (temporary storage) but inhibit read in to ER
9. Write ER in 0-2
10. Read out 0-1 (AC) to ER
11. Rewrite
12. Sense ~~information~~ in ER for negative sign, if negative then continue, otherwise change back to program timing.

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13. Read out 0-2 to ER
14. Rewrite* (to reset cores in selection switch)
15. Read out 0-0 (PC) but inhibit read in to ER
16. Write ER in 0-0 (PC)

Steps not shown to leave previous contents of PC in AR, but this presents no difficulty and indeed does not increase the number of transfers to storage.

mr

Operation timing shown below preceded by program timing.
Ten digit number assumed

8. Read out selected register to ER
9. Rewrite
10. Clear 0-5 to 0-15 if necessary. (These registers may be left clear at completion of order and unless possibility exist that they may contain information from previous orders do not have to be cleared.)
11. Transfer ER into 0-5 to 0-15
12. Clear ER
13. Read out 0-1 to ER (AC containing multiplier.)
14. Rewrite*
15. Clear 0-5 if digit 11 in ER is a zero
16. Rewrite* (must be zero rewrite)
17. Shift right one
18. Clear 0-6 if digit 11 in ER is a zero
- .
- .
- .
- . repeat through 0-14
- .
- .

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- 45. Clear ER
- 46. Read out 0-5 to ER
- 47. Rewrite* (could be zero rewrite to leave registers clear)
- 48. Shift right one
- 49. Read out 0-6
 - .
 - .
 - : repeat through 0-13
 - .
 - .
- 73. Read out 0-14 to ER
- 74. Rewrite*

The cyclic parts such as clearing and reading into registers 0-5 to 0-15, or reading out of progressive registers may be accomplished by a repeating of the time pulses but adding one to the storage selection switch at the end of each cycle.

Four storage operations, a read and a write, are necessary for the clear and add order. The storage operations for the other orders shown are: transfer to storage, 4; conditional program, 6; multiply and round off, 34 for a ten digit number or three times the number of digits plus four.

Signed B. E. Morriss
B. E. Morriss

Approved Jay W. Forrester
Jay W. Forrester

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