Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BI-WEEKLY REPORT, PART I, APRIL 1, 1949

To: 6345 Engineers

From: Jay W. Forrester

## 1.0 WHIRLWIND I COMPUTER ELEMENTS

### 1.01 Production Report

(H. F. Mercer)

During the past two weeks we have received from Sylvania the following panels (production units):

8 Flip-Flop Storage Registers

During the same period we completed here:

Clock Pulse Control

### 1.02 WWI System

(N. H. Taylor)

The system was put back in operation during the last week after a three-week shutdown for power wiring modifications.

The problems arising during the first few hours of operation were unique and are treated in Memorandum M-820. The most perplexing problems resulted from stray pulses being generated in the system, due to the omission of bias in a particular rack of equipment. A tube loose in its socket in one of the control circuits also caused considerable delay in getting the system going.

During the last three-month period, we have run the computer about 300 hours and during this time, we have lost none of our flip-flop or gate tubes even though they have been turned on and off frequently. Our only tube failures to date have been two indicator tubes, due to internal short circuits.

1.02 WWI System (continued)

(G. C. Sumner)

System testing was resumed March 28 after a three-week period of installation. Operation was resumed after only minor difficulties. It was found that some signal amplitudes were not the same as they had been set some weeks previous, especially in the test control. This indicated that a general check of amplitudes should be made. That is now being done and will be completed the first of next week.

Marginal checking equipment has been given a preliminary test. One flip-flop was found to have a very low margin. The details of WWI marginal checking will occupy a large portion of test time in the near future.

1.1 Listed by System Number

103 Program Register

(H. Fahnestock)

Designs have been completed for modifications to the program register to enable it to function as the flip-flop register for electrostatic storage. The block schematic is B-39289-2, the circuit schematic is D-33836.

104 Control Sw./Storage Sw.

(C. W. Watt)

Switch Panel: Assembly work is well along - about one week ahead of schedule.

Matrix Panel: Drafting is nearly finished.

Output Panel: Fabrication of sheet metal is completed.

106 Time Pulse Distributor

(K. E. McVicar)

Tests on the time pulse distributor counter and output panels are nearing completion. The output panel has just returned from the shop where modifications were made, and the counter panel will be modified early next week. After final modification the panels will be checked again and in the meantime test specs have been started.

109 Clock Pulse Control

(R. H. Gould)

Resistance measurements on the CPC panel discovered a faulty crystal diode and a faulty choke which were replaced. Dynamic testing of the flip-flops has shown that rise and fall times with cathode triggering are a maximum of .25 microseconds. The important time of complete switching of the gate tubes after an input to a flip-flop grid will be measured.

Redesign of CPC is being considered to provide for constant frequency restoration by stopping computer operation at regular intervals.

111 Synchronizer

(H. S. Lee)

The wiring of the terminal board and fabrication of the panel cabling has been completed. The final assembly has been started but suspended temporarily pending completion of more urgent projects. This temporary suspension will not effect the schedule as the panel is presently four and one-half weeks ahead of schedule.

202 Toggle Switch Storage Output Panel

(C. W. Watt)

Final assembly is about 1/2 done. Three and one-half weeks ahead of schedule.

Toggle switch storage switch panel sheet metal is nearly complete.

204 Electrostatic Storage Control

(H. Fahnestock)

The design for electrostatic storage control is described by Dodd, Taylor, Everett, O'Brien and Mayer in E-219.

404 Comparison Register Check

(H. S. Lee)

The video layout is approximately 75% completed.

404 Comparison Register Check (continued)

The mechanical detail of the aluminum panel should be completed by April 5.

500 Input-Output Control

(J. A. O'Brien)

The preliminary study of the block diagram of input-output control has been completed. The notes made during this study with a few explanatory paragraphs have been written up in a memo, M-818, including a sketch of the block diagram.

It is expected that several changes will be made in the diagram before the actual design proceeds much further.

The problem of driving signals to the various units involved has been considered and it seems that the register drivers in the flip-flop storage row will be adequate.

(A. K. Susskind)

The design of input-output control, based on block schematic SD-33818, has been started.

1.2 System Engineering

(C. W. Watt)

Installation - Power was turned on the racks on Monday, March 28, for the first time since March 7. During the day various difficulties were corrected and by Tuesday the power distribution system was operating properly.

Installation is now being continued on flip-flop storage racks F0-F15, the voltage variation racks P6-P14, the flip-flop register driver rack, FD, and control rack C12.

1.21 Power Control and Distribution

(H. S. Lee)

Voltage Variation Panels: It has been decided that Sylvania will not assemble any of the voltage variation panels. Our shop has started assembly of four panels and the remainder will be completed as slack time fill-in projects.

1.22 Power Cabling

(H. S. Lee)

Drafting of the power cables for rack C13 has been completed and a construction requisition forwarded to the shop for fabrication.

Fabrication of cables for rack C12 is 80% complete and installation of the completed cables has started.

Drafting of cables for rack C8 is 90% complete.

It is planned to employ additional drafting personnel on power cables in the very near future in order to advance the cabling schedules to conform to the advanced completion dates of the control panels.

1.23 Video Cabling

(R. H. Murch)

Video cable master schedules have been completed, except for checking, on all cables measured by M.I.T. Assembly drawings for these cables have been completed but also unchecked.

A drawing (E-33705) showing flip-flop storage register driver assignments has been drawn and issued. A video cabling block schematic of flip-flop storage is being drawn.

1.24 Driver Panels

(W. N. Papian)

Standardizer Amplifier: This unit is as described in M-812 (March 24, 1949). Only minor changes were made to the circuitry of the two stages which were lifted from the pulse standardizer (C-33001-2).

Rough results are as follows: negligible p.r.f. sensitivity up to 2 mc; negligible output for jack inputs under 1 volt; unreliable output for jack inputs from 1 volt to about 2 or 3 volts; almost standard jack output of about 29 volts for jack inputs of 3 volts and up.

The circuit schematic has been turned over to drafting; and a rough suggested layout for a $9\frac{1}{2}$" WWI panel to contain 5 of these channels is in preparation.

1.25 Time Schedules

(R. A. Osborne)

The summary schedule for February's Summary Report was posted.

All detailed schedules are in the process of being posted for March. Schedules should be distributed to interested parties late next week.

1.3 Auxiliary Equipment

1.31 Power Supplies

(C. R. Wieser)

The filament-control panel has been tested and found satisfactory. It will be connected to the system as soon as the filament voltage regulator is completed.

The thermal time-delay relays in the d-c supplies have been found unsatisfactory since they are reset when the supplies are running. If the computer is switched to "Standby" and then quickly turned "ON" the d-c voltages will be delayed and come on in random sequence. This has been temporarily corrected by installing a time delay in the "ON" circuit. Arrangements have been made with Power Equipment Co. to replace the thermal relays with motor driven timers which will not have to be reset while the supplies are in operation.

The two unused phases of the 31 kva, 3-phase alternator (now feeding WWI filaments) have been connected to the Storage Tube Demonstrator to furnish power free from transients.

Construction of a bread-board regulator for the WWI filament alternator has been started. A power supply for the regulator is also under construction.

(J. J. Gano)

WWI D-C Power: The damping of the regulators on the +250 and +150 supplies was adjusted according to observations of transients on the Brush Oscillograph upon sudden application of load. The other supplies will be adjusted when there will be no interference with computer operation.

1.31 Power Supplies (continued)

WWI Filament Power: Time constants on the exciter and alternator were secured. A bread-board assembly of the regulator is underway.

| WWI Drawing List | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| System | B-37071-5 | | |
| Control | B-37098-4 | | |
| Master Clock | B-37159-2 | | |
| 101 Pulse Generator | B-37155-3 | B-32385 | E-32333-4 |
| 102 Program Counter | B-37062-4 | B-32213-1 | D-31516-6 |
| 103 Program Register | B-37067-3 | B-39289-2 | D-33836 |
| 104 Control-Switch Matrix Panel | B-37066-3 | C-33843 | R-32722-2 |
| 104 Control-Switch Switch Panel | B-37066-3 | | Z60CS00-2-C |
| 104 Control-Switch Output Panel | B-37066-3 | | Z60CS00-A |
| 105 Operation Matrix Driver Panel | | S600M00 | Z600M00-1-E |
| 105 Control-Pulse Output | | R60CP00 | S60CP00-1-B |
| 106 Time-Pulse Distributor | B-37068-4 | T60PD00-3-A<br>T60PD00-4-B | |
| 106 Time-Pulse-Distributor Counter | | T60PD00-3-A | Y60PD00-C |
| 106 Time-Pulse-Distributor Output | | T60PD00-4-B | Z60PD00-1-D |
| 109 Clock-Pulse Control | B-39817-3 | C-32642-4 | R-31916-7 |
| 110 Frequency Divider | B-37154-3 | B-32264-1 | R-31729-2 |
| 111 Synchronizer | B-37172 | C-33485 | R-33486-1 |
| 112 Restorer-Pulse Generator | B-37160-1 | B-32209-4 | D-31909-8 |
| 200 Storage | B-37156-2 | | |
| 201 Test-Storage Amplifiers | B-37121-2 | B-32855-2<br>C-33768 | D-33706 |
| 201 Storage-Switch Matrix Panel | B-37121-2 | C-32855-3 | R-32722-2<br>D-33706 |
| 201 Storage-Switch Switch Panel | B-37121-2 | | Z60CS00-2-C |
| 201 Storage-Switch Output Panel | B-37121-2 | | Z60CS00-A |

| WWI Drawing List (Continued) | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| 202 Toggle-Switch-Storage Switch Panel | B-37122-3 | C-33768 | D-33706<br>C-33707 |
| 202 Toggle-Switch-Storage Output Panel | B-37122-3 | | E-32721-3 |
| 203 Flip-Flop-Storage Output | B-37060-5 | B-32269-1 | E-31635-4 |
| 203 Flip-Flop Storage Register | B-37057-4 | B-32268-1 | E-31621-4 |
| 203 Flip-Flop Storage Control | B-37061-7 | D-32106-2 | |
| 301 A-Register, Digits 1-15 | B-37056-3 | B-31211-3 | D-31276-11 |
| 301 A-Register, Digit 0 | B-37056-3<br>B-37072-7 | B-31574-1 | D-31573-7 |
| 302 Accumulator, Digits 1-14 | B-37173 | D-31213-3 | R-31275-9 |
| 302 Accumulator, Digit 0 | B-37173 | D-32851 | R-32850-2 |
| 302 Accumulator, Digit 0, Aux. Panel | B-37173 | B-32492-2 | D-32602-1 |
| 303 B-Register | B-37097-4 | B-31212-5 | D-31277-6 |
| 304 Sign Control &<br>308 Divide-Error Control | B-37072-7 | C-31576-3 | E-31619-2 |
| 305 Step-Counter | B-37074-6 | D-31828-1 | D-39764-3 |
| 305 Step-Counter Output | | A-32723-1 | D-32735-2 |
| 306 Multiply &<br>307 Shift Control | B-37072-7 | C-31532-3 | E-31588-5 |
| 308 Divide Control | B-37072-7 | C-31552-3 | R-31718-5 |
| 309 Special Add Memory & ACO Carry | B-37072-7 | C-31575-4 | E-31632-4 |
| 310 Point-Off Control | B-37072-7 | C-31600-6 | E-31717-6 |
| 403 In-Out Register | B-37119-2 | B-32434-2 | D-31277-6 |
| 404 Comparison Register | B-37120-2 | B-32578-1 | E-32576-5 |
| 404 Comparison-Register Check | | B-33488-1 | E-33515 |
| 601 Check Register | B-39816-3 | B-32577-1 | E-32576-5 |
| 601 Check-Register Check | | B-32018-1 | E-32023-2 |

| WWI Drawing List (continued) | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| Alarm Indicator Control | B-37175 | B-33603 | E-33651 |
| Bus Connections | B-37124-3 | C-37123-3 | |
| Bus Driver, Arithmetic Element | | A-32297-1 | D-31727-7 |
| Bus Driver, Flip-Flop Storage | | A-32296-1 | D-31726-7 |
| Register Driver, Type I | | B-32207-1 | E-32261-7 |
| Register Driver, Type II | | B-32691-2 | D-32690-2 |
| Fuse-Indication Panel | | | W60PP00-7-D |
| Voltage-Variation Panel | | | W60PP00-6-C |
| WWI Power-Connector Pin Connections | | | B-31955-6 |
| Digit-Interlock Panel | | | W60PP00-8-B |
| Fixed-Voltage Switching Panel | | | T-60PP00-11-B |
| Power-Interlock & Indication Panel | | | Z-60PP00-12-A |

## 2.0 WHIRLWIND I RESEARCH

### 2.2 Components

#### 2.23 Vacuum Tube Studies

(H. B. Frost)

A group of weak 6AS6 tubes from the multiplier were pulse tested. These tubes have badly deteriorated cathodes, with no interface. Poor operation is caused by temperature limiting of emission. An engineering note is being prepared on these tubes.

Some work has been done with John Weymouth in the problem of quantitative measurement of interface resistance. Some progress has been made, but exact correlation of results is lacking.

The prototype Multivibrator Frequency Divider is now being used in the life test racks.

Life tests have been started on 5687 tubes and 7AD7 tubes (F8B), the 7AD7's with low filament voltage.

(R. L. Ellis)

Seventy-five 5687 tubes of a new production number, 3229-13, have been received and given the laboratory standard tests. Five tubes failed. Four others are being investigated further.

Seven 3E29 tubes have been returned recently as failures. Tests show all have developed high gas content. The tubes have been operated but a few hours.

Families of plate and screen current versus screen voltage curves made by varying both suppressor and control-grid voltages have been completed for 7AK7's. The drawing numbers are A-40493 through A-40500.

All requests to date for tube components are filled and a reasonable reserve of tested tubes of all types are available.

## 2.3 Systems

### 2.31 Five-Digit Multiplier

(R. W. Read)

Extensive work has been done in the past two weeks to bring the multiplier to the performance it had previously shown. However, the 15 volt bias is obtained through a simple regulator from the -150 lab supply; there is evidence that serious errors and even continuous errors can be introduced into the multiplier by surges on either of two of the lab D.C. supplies.

A more vigorous account of errors and bad time was started on March 23. The pattern of error sources hinted that many 6AS6 (G.T.) with over about 3000 hours had failed. Since the retests of February 28 did not support this indication, another test was made, at 5 volts on the filaments, as suggested by Frost; all tubes which deviated far below the norm were rejected. About one-half of the tubes tested were rejected. The retest of February 28, which approximated JAN specifications, showed all tubes to have between 70 and 100% original omission.

From March 23 until April 1, a total of 140 hours of good time were recorded. About 70 hours was noted as bad time, including marginal checking and service time. During this period about 15 6AS6's were retired, 3 7AD7's and 1 7AK7.

## 4.0 BLOCK DIAGRAMS

(R. R. Everett)

The following memoranda have been issued in cooperation with the circuits group:

M-818 In-Out Control
M-219 Electrostatic Storage Control

While these reports are not entirely complete or final, they do form a working basis from which design can proceed.

(R. P. Mayer)

Timing for the use of the Program Register as the Electrostatic Storage Output Register has been worked out. This work has also been expanded to provide for coordination between the operations of Test Storage and Electrostatic Storage. A block diagram has been designed for providing automatic selection of TS or ES during normal high-speed operation of WWI. This diagram follows the timing and coordination schemes mentioned above, and can probably be obtained by using one BR panel and two ACO Auxiliary panels.

(J. M. Salzer)

A preliminary block diagram on the Input-Output (including registers, checking and control), SD-37178, has been issued. It supplements Memorandum M-818 and Block Schematic SD-33818.

The timing of the six input-output orders has been worked out and integrated with ES operation. A note on these and on input-output checking is in preparation.

## 5.0 CHECKING METHODS

(N.H.Taylor)

The recent power wiring modifications have made possible a limited amount of marginal checking activity.

At present we are able to check the flip-flop tubes in the same manner as we have used in the Five-Digit Multiplier. We can also vary the voltage on the screens of the gate tubes in the repetitive racks, as well as in arithmetic control.

We will begin to collect data on voltage variation of these elements of the computer on a day by day schedule. From this experience we will find the most effective way to use this marginal checking equipment.

(G.Cooper)

The work on demonstration problems has been more or less completed. That is, all problems which have occurred to me have been investigated. It may be that there are other interesting types of problems within the capacity of test storage. The results of this work have been written up and will soon be published (E-220).

Consideration has been given to an approach to coding which makes use of successive modifications of the operation section of each order (perhaps with some modification of the address section, too). It may be safely said that this method does not have any advantages in general. It has been applied to a checking problem devised by C. W. Adams and has been found to require considerably more storage than a straightforward program. In addition, it was applied to a checking problem which I devised. Once again, it exceeded the capacity of test storage, whereas the straightforward program did not. Further, in order to apply this technique, a certain numbering of the operation codes is required. This numbering requirement differs from problem to problem. It may be concluded that this technique is not generally useful, though a limited application of it may sometimes save on storage requirements.

(C.W.Adams)

During the past two weeks various aspects of checking have been considered and discussed with interested parties. At present little thought is given to the routine spot-check problems which will be used during normal operation; rather, the problem of checking equipment and locating trouble as new units are added to the system and

5.0 CHECKING METHODS (cont)

the problem of testing the reliability of the system are receiving attention. The subject can be subdivided into the three slightly overlapping problems enumerated below.

1) At the suggestion of G. Sumner programs are being worked out which will facilitate the initial checking and trouble location of WWI control, test storage, and check register immediately after their installation. It is planned to extend the technique now used for checking the arithmetic element to the larger system. That is, it will be possible by the use of delay-counting elements (perhaps using digits of the program counter which are not needed in operation with test storage) to stop the computer on any time pulse of any operation of a repeating program (stored in test storage) long enough for the indicator lights to show the condition of all flip-flops after that particular time pulse. In this way the effect of each pulse of a fairly long test sequence can be examined. A simple and direct program which seems to check all of control, test storage, and the check register has been written. It uses all of the sixteen definitely approved orders and repeats none of them. This program actually checks part of the arithmetic element as well as control, and may be adaptable to a complete check of the computer, but for the present purpose the arithmetic element will be considered essentially trouble-free and the interest will be focussed on checking control.

2) The question of checking the arithmetic element under WWI control, and in particular checking for prf sensitivity, may be facilitated by some special operations which would not normally be used in final operation, as well as by some of the operations which may become standard but which cannot be adopted for final design until more experience has been obtained both in their usefulness and in the need for other operations which might become urgent. In the first category, operations can be designed, using existing equipment; (1) to multiply repeatedly, say four or eight times, as one operation; (2) to divide and then shift-left-fifteen as one operation; (3) to divide and shift left repeatedly as in multiplication. In the second category, it may be convenient to wire in, temporarily, the ro, as, ao, and at operations which have been suggested, discussed, but not definitely accepted.

3) The problem of reliability testing after successful operation of the system has been achieved, but before much useful work is undertaken (particularly before electrostatic storage and input-output are completely available) can be handled partly by repeated

5.0 CHECKING METHODS (cont.)

performance, self-checked, of the type of programs used for initial testing if they can be adapted to provide a more complete check of the arithmetic element. Another possibility which is inefficient and may appear at first glance slightly ludicrous but which might be interesting and perhaps reassuring is to require the computer to perform every possible multiplication and division. Evidently, since $2^{15}$ different numbers can be distinguished in the computer, disregarding sign, $2^{30}$ (minus $2^{15}$ to prevent duplication of terms of the form a.a) or about one billion multiplications, and about half as many divisions, would be required. This process has been programmed preliminarily without regard for the time required but with self-checking of the results. In its present form, the program (which easily fits into test storage) will keep the computer occupied for a little over three days. While this time can undoubtedly be reduced perhaps one day or so, the three day task is not unreasonable to talk about. Labor Day weekend might be an ideal time to try it out.